

Compal confidential

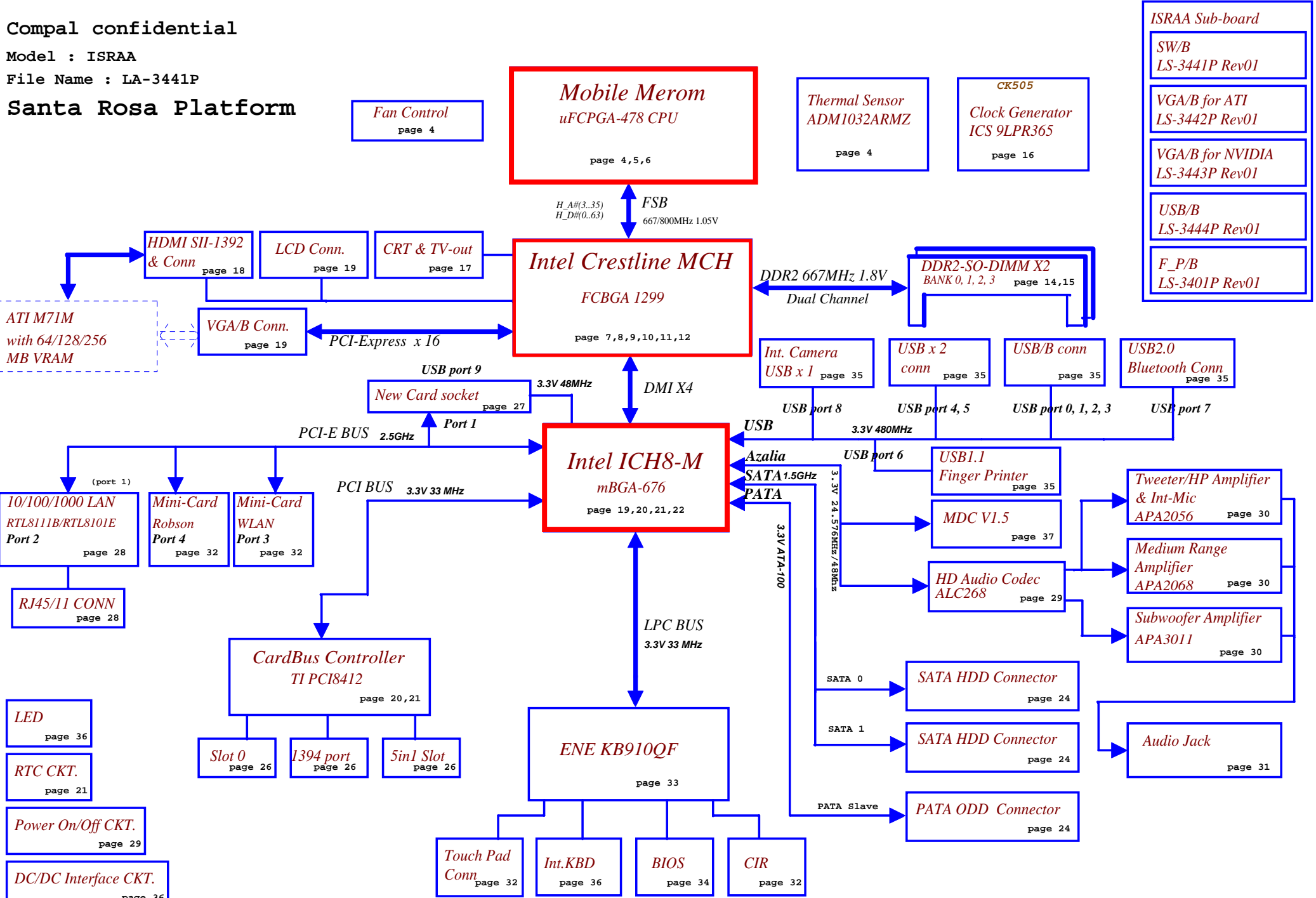
ISRAA LA-3441P Schematics Document

Mobile Merom uFCPGA with Intel
Crestline_PM+ICH8-M core logic

2006-09-21

REV:0.1

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Issued Date	2006/06/30	Deciphered Date	2007/06/30	Cover Sheet		
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				Custom	ISRAA LA-3441P	0.1
				Date:	Friday, September 22, 2006	Sheet 1 of 48



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				Document Number	0.1
				Date:	Thursday, September 21, 2006
				Sheet	2 of 48

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Block Diagram

Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05Vs	1.05V power rail for Processor I/O and MCH/ICH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+1.25Vs	1.25Vs power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD20	2	A,B,C
CARD BUS	D4	AD20	2	A,B,C
SIN1	D4	AD20	2	A,B,C

KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1010000 X b
SM1 SMART BATTERY	16H	0001011 X b
SM2 ADM0132	98H	1001100 X b
CPU THERMAL MONITOR		

ICH8-M SM Bus address

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1010000
DDR SO-DIMM 1	A4	1010010
CLOCK GENERATOR (EXT.)	D2	11010010

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 1%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0.100 V
1	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
2	18K +/- 1%	0.436 V	0.503 V	0.538 V
3	33K +/- 1%	0.712 V	0.819 V	0.875 V
4	56K +/- 1%	1.036 V	1.185 V	1.264 V
5	100K +/- 1%	1.453 V	1.650 V	1.759 V
6	200K +/- 1%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	10
1	10G
2	10H
3	
4	
5	
6	
7	

BTO Option Table

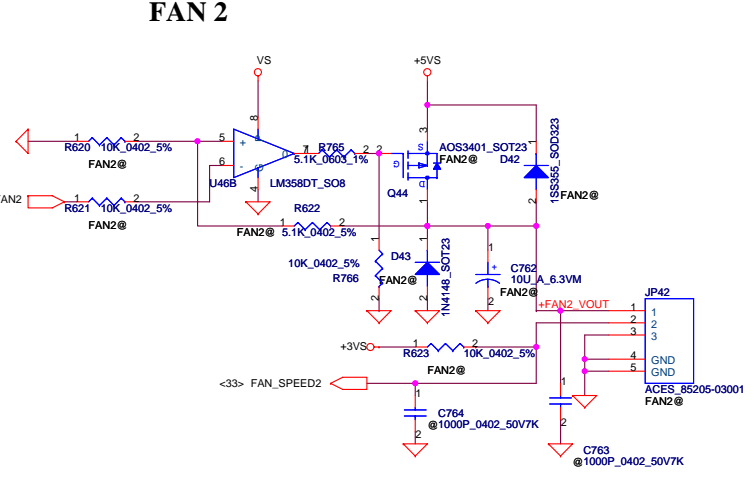
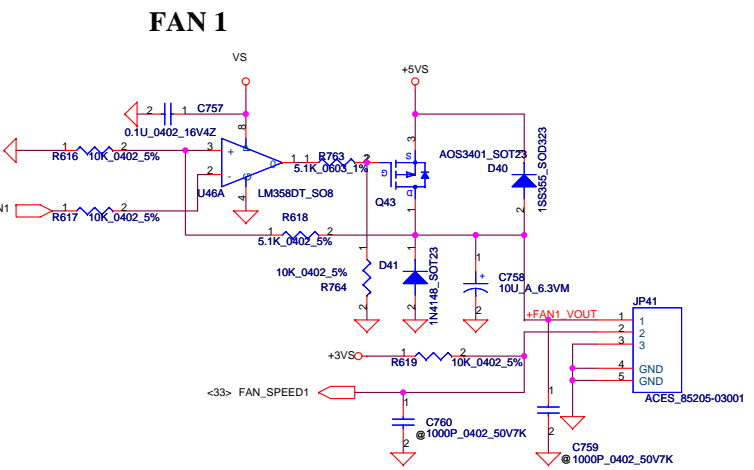
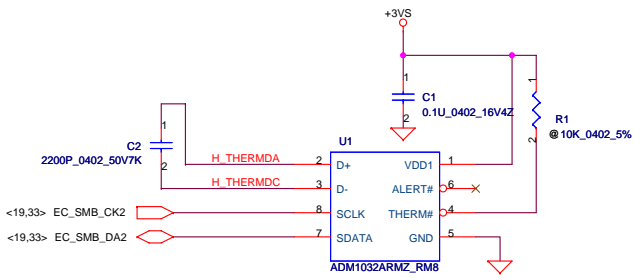
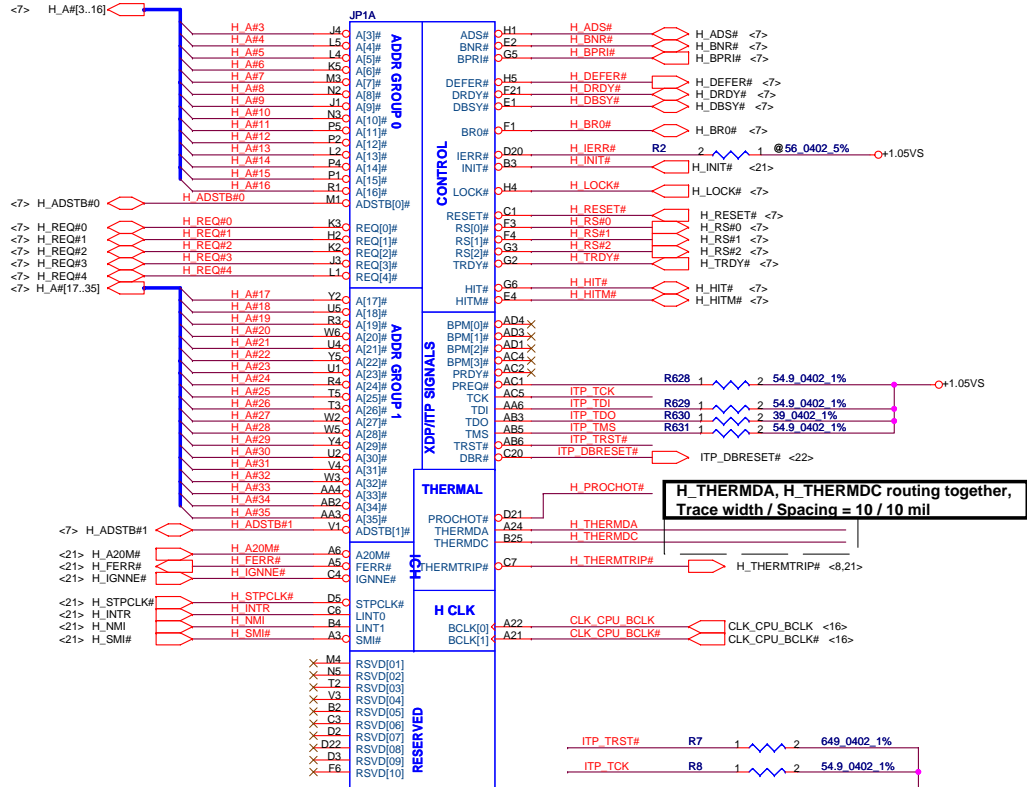
BTO Item	BOM Structure
2ND HDD	2HDD@
LAN	100M@ 1000M@
WLAN	WLAN@
NB	GM@ PM@
BT	BT@
MIC	MIC@
CIR	CIR@
FINGER PRINT	FP@
Express Card	NEWCARD@
PCMCIA Card	PCMCIA@
Camera	Camera@
Robson	Robson@
HDMI	1392@ 1932@ M72M@
SPEAKER	

USB PORT LIST

PORT	DEVICE
0	RIGHT USB Port (Samll Board)
1	RIGHT USB Port (Samll Board)
2	RIGHT USB Port (Samll Board)
3	RIGHT USB Port (Samll Board)
4	LEFT USB Port
5	LEFT USB Port
6	Fingerprint
7	Blue Tooth
8	Internal Camera
9	Express Card

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Date: Thursday, September 21, 2006				Sheet 3 of 48

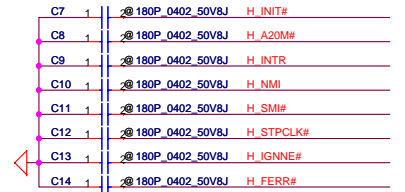
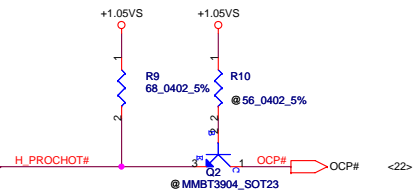
Thermal Sensor ADM1032ARM



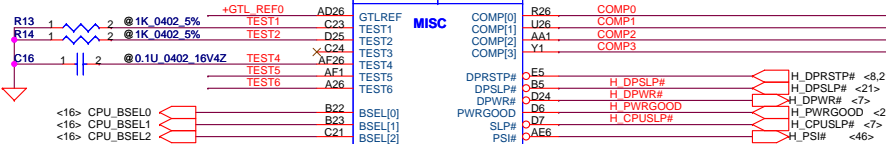
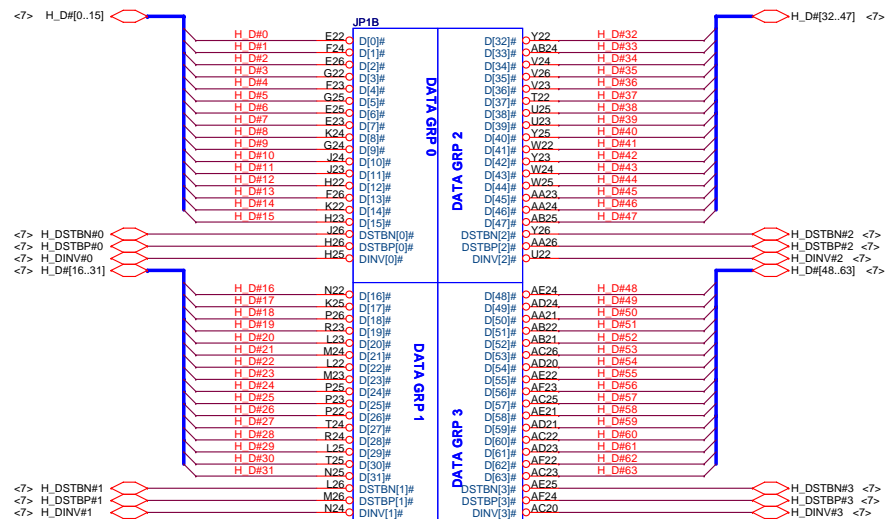
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H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

Place Caps Close to CPU Socket



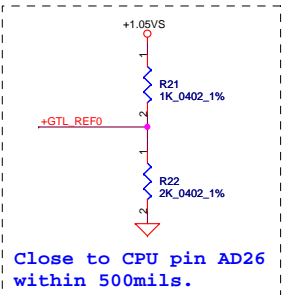
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			Date:	Friday, September 22, 2006	Sheet 4 of 48



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs
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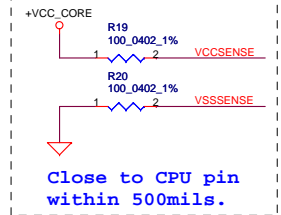
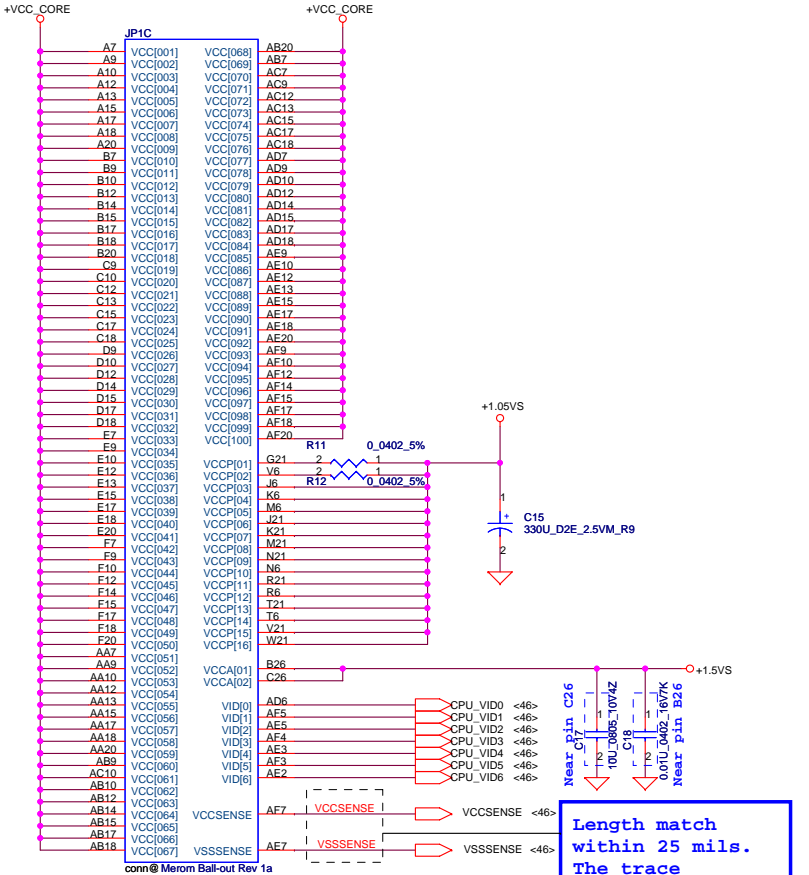
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



+GTL_REF0 Impedance control 55 Ohm

Close to CPU pin AD26 within 500mils.

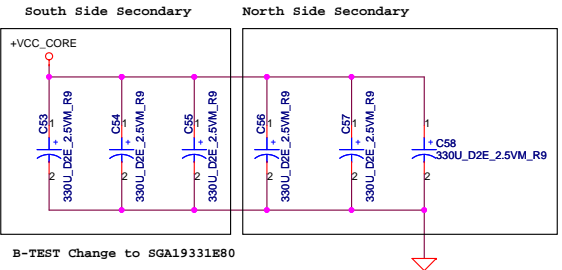
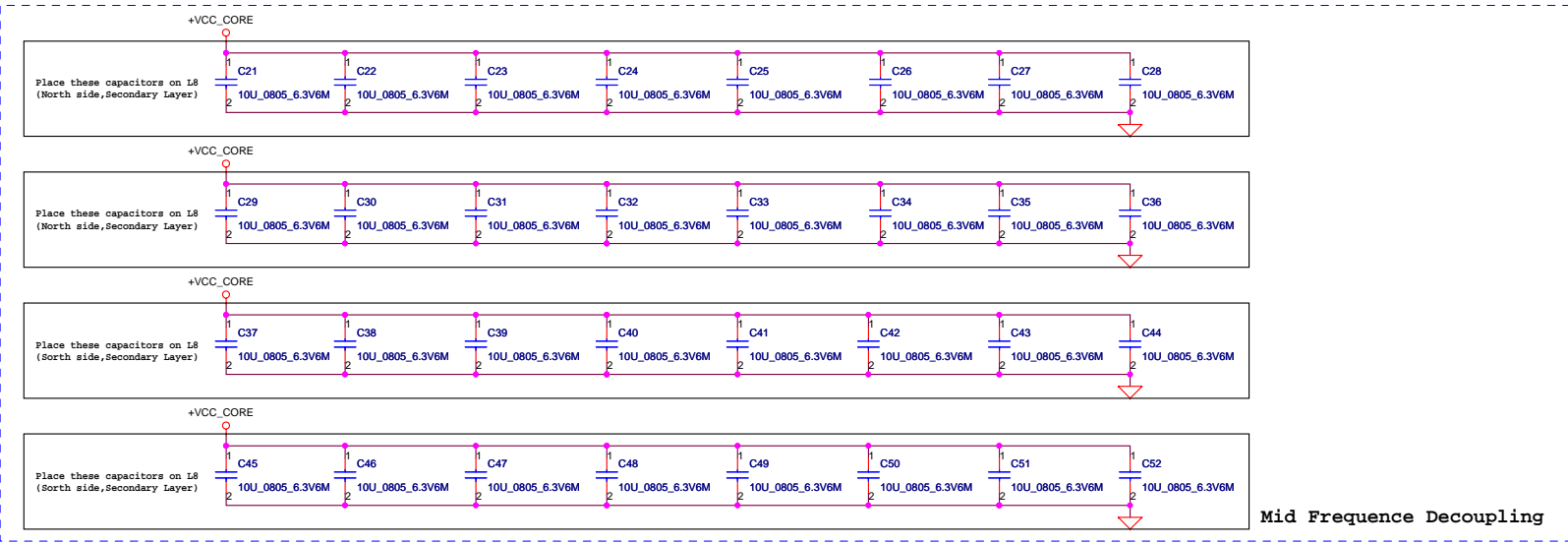


Close to CPU pin within 500mils.

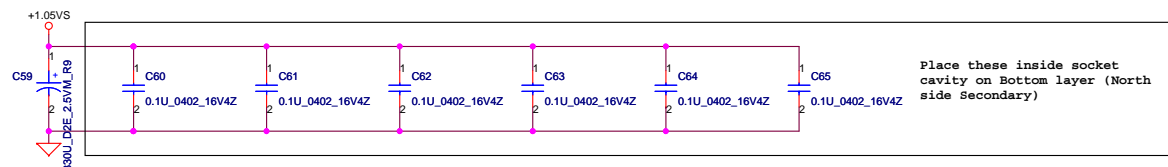
Length match within 25 mils. The trace width/space/other is 20/7/25.

JP1D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
AF2	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B12	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C6	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C19	VSS[021]	VSS[102]
C16	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C22	VSS[024]	VSS[105]
D1	VSS[025]	VSS[106]
D4	VSS[026]	VSS[107]
D8	VSS[027]	VSS[108]
D9	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D16	VSS[030]	VSS[111]
D19	VSS[031]	VSS[112]
D23	VSS[032]	VSS[113]
D28	VSS[033]	VSS[114]
E3	VSS[034]	VSS[115]
E6	VSS[035]	VSS[116]
E8	VSS[036]	VSS[117]
E11	VSS[037]	VSS[118]
E14	VSS[038]	VSS[119]
E16	VSS[039]	VSS[120]
E19	VSS[040]	VSS[121]
E24	VSS[041]	VSS[122]
F2	VSS[042]	VSS[123]
F5	VSS[043]	VSS[124]
F8	VSS[044]	VSS[125]
F11	VSS[045]	VSS[126]
F13	VSS[046]	VSS[127]
F16	VSS[047]	VSS[128]
F19	VSS[048]	VSS[129]
F22	VSS[049]	VSS[130]
F25	VSS[050]	VSS[131]
G4	VSS[051]	VSS[132]
G1	VSS[052]	VSS[133]
G26	VSS[053]	VSS[134]
H3	VSS[054]	VSS[135]
H6	VSS[055]	VSS[136]
H21	VSS[056]	VSS[137]
H24	VSS[057]	VSS[138]
J2	VSS[058]	VSS[139]
J5	VSS[059]	VSS[140]
J22	VSS[060]	VSS[141]
J25	VSS[061]	VSS[142]
K1	VSS[062]	VSS[143]
K23	VSS[063]	VSS[144]
K26	VSS[064]	VSS[145]
L3	VSS[065]	VSS[146]
L6	VSS[066]	VSS[147]
L21	VSS[067]	VSS[148]
L24	VSS[068]	VSS[149]
M2	VSS[069]	VSS[150]
M5	VSS[070]	VSS[151]
M22	VSS[071]	VSS[152]
M25	VSS[072]	VSS[153]
N1	VSS[073]	VSS[154]
N4	VSS[074]	VSS[155]
N23	VSS[075]	VSS[156]
N26	VSS[076]	VSS[157]
P3	VSS[077]	VSS[158]
	VSS[078]	VSS[159]
	VSS[079]	VSS[160]
	VSS[080]	VSS[161]
	VSS[081]	VSS[162]
		VSS[163]
		AF25

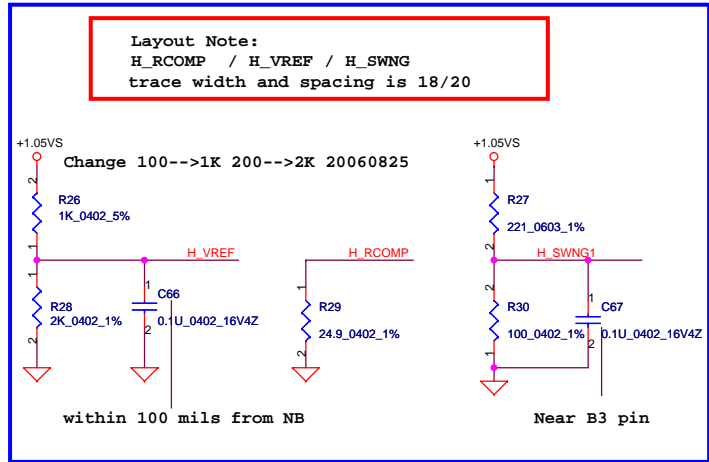
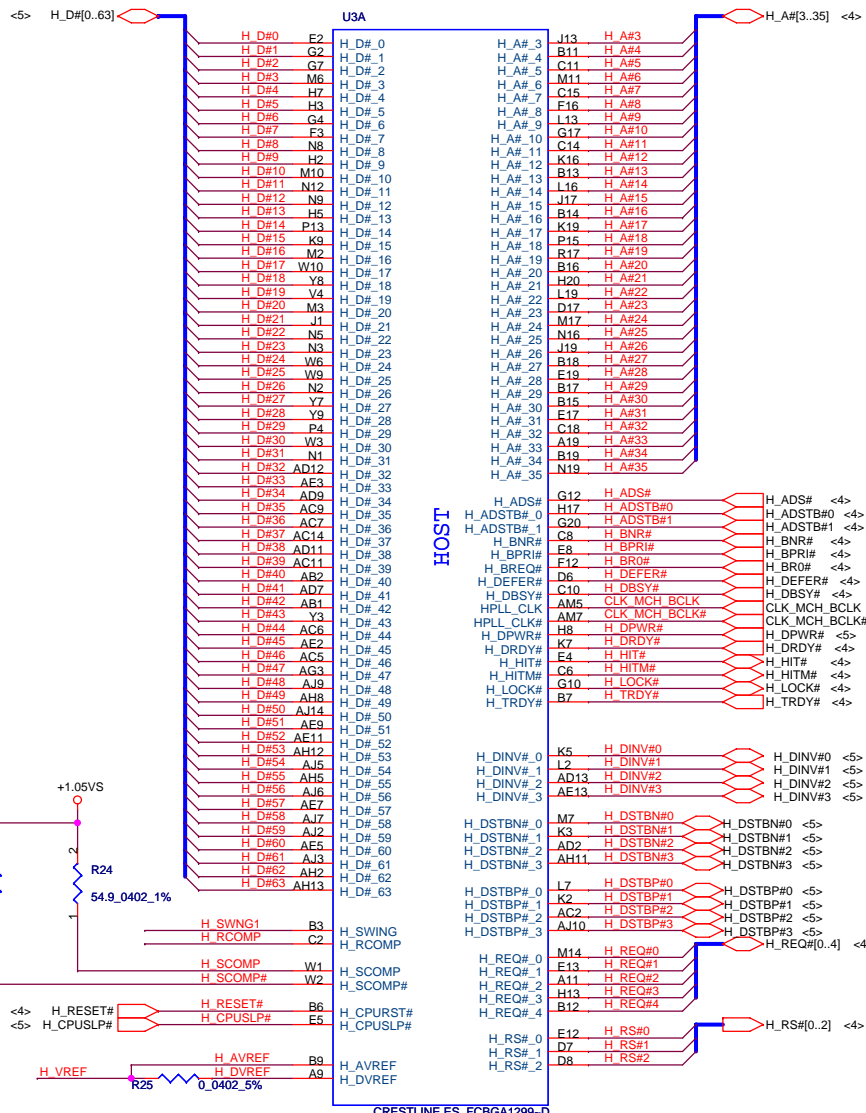
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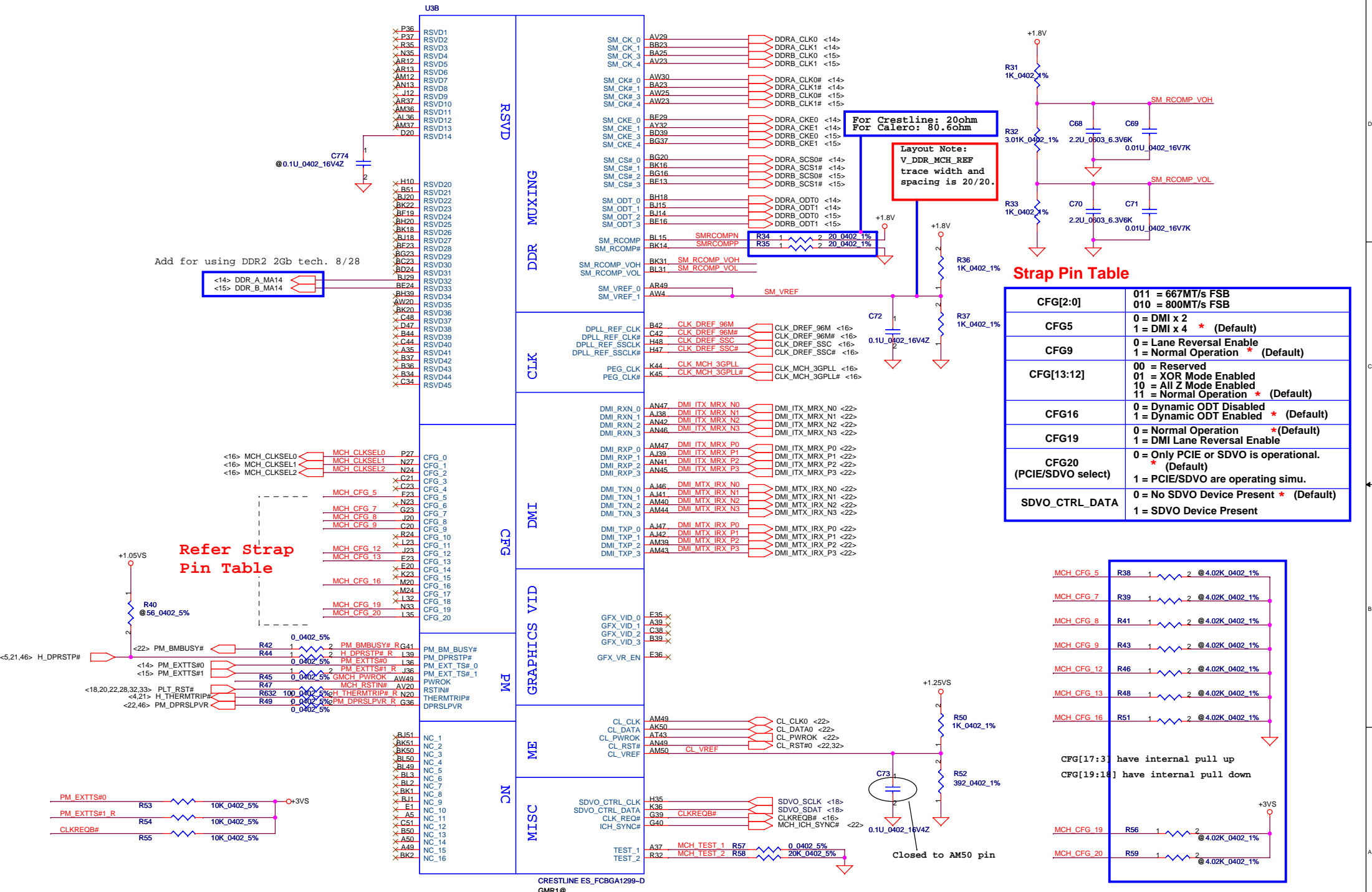
ESR <= 1.5m ohm
Capacitor > 1980uF
330uF ESR 7m ohm X 6 PCS



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				Custom	ISRAA LA-3441P	0.1
				Date:	Thursday, September 21, 2006	Sheet 6 of 48



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Size	Document Number	ISRAA LA-3441P		Rev	
B				0.1	
Date:	Friday, September 22, 2006	Sheet	7	of 48	



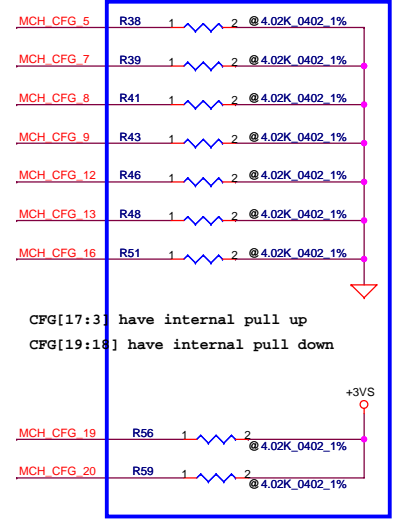
For Crestline: 20ohm
For Calero: 80.6ohm

Layout Note:
V_DDR_MCH_REF
trace width and
spacing is 20/20.

Strap Pin Table

CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. * (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRL_DATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present

Refer Strap Pin Table



<14> DDRA_SDQ[0..63] DDRA_SDQ[0..63]

<14> DDRA_SDM[0..7] DDRA_SDM[0..7]

<14> DDRA_SMA[0..13] DDRA_SMA[0..13]

<15> DDRB_SDQ[0..63] DDRB_SDQ[0..63]

<15> DDRB_SDM[0..7] DDRB_SDM[0..7]

<15> DDRB_SMA[0..13] DDRB_SMA[0..13]

U3D

DDRA_SDQ0 AR43 SA_DQ_0

DDRA_SDQ1 AW44 SA_DQ_1

DDRA_SDQ2 BA45 SA_DQ_2

DDRA_SDQ3 AY46 SA_DQ_3

DDRA_SDQ4 AR41 SA_DQ_4

DDRA_SDQ5 AR41 SA_DQ_5

DDRA_SDQ6 AT42 SA_DQ_6

DDRA_SDQ7 AW47 SA_DQ_7

DDRA_SDQ8 BB45 SA_DQ_8

DDRA_SDQ9 BF48 SA_DQ_9

DDRA_SDQ10 BG47 SA_DQ_10

DDRA_SDQ11 B145 SA_DQ_11

DDRA_SDQ12 BB47 SA_DQ_12

DDRA_SDQ13 BG50 SA_DQ_13

DDRA_SDQ14 BH49 SA_DQ_14

DDRA_SDQ15 BE45 SA_DQ_15

DDRA_SDQ16 AW43 SA_DQ_16

DDRA_SDQ17 BE44 SA_DQ_17

DDRA_SDQ18 BG42 SA_DQ_18

DDRA_SDQ19 BE40 SA_DQ_19

DDRA_SDQ20 BF44 SA_DQ_20

DDRA_SDQ21 BH45 SA_DQ_21

DDRA_SDQ22 BG40 SA_DQ_22

DDRA_SDQ24 BF40 SA_DQ_23

DDRA_SDQ25 AR40 SA_DQ_24

DDRA_SDQ26 AT39 SA_DQ_25

DDRA_SDQ27 AW36 SA_DQ_26

DDRA_SDQ28 AW41 SA_DQ_27

DDRA_SDQ29 AY41 SA_DQ_28

DDRA_SDQ30 AV38 SA_DQ_29

DDRA_SDQ31 AT38 SA_DQ_30

DDRA_SDQ32 AV13 SA_DQ_31

DDRA_SDQ33 AT13 SA_DQ_32

DDRA_SDQ34 AW11 SA_DQ_33

DDRA_SDQ35 AV11 SA_DQ_34

DDRA_SDQ36 AU15 SA_DQ_35

DDRA_SDQ37 AT11 SA_DQ_36

DDRA_SDQ38 BA13 SA_DQ_37

DDRA_SDQ39 BA11 SA_DQ_38

DDRA_SDQ40 BE10 SA_DQ_39

DDRA_SDQ41 BD10 SA_DQ_40

DDRA_SDQ42 BD8 SA_DQ_41

DDRA_SDQ43 AY9 SA_DQ_42

DDRA_SDQ44 BG10 SA_DQ_43

DDRA_SDQ45 AW9 SA_DQ_44

DDRA_SDQ46 BD7 SA_DQ_45

DDRA_SDQ47 BB9 SA_DQ_46

DDRA_SDQ48 BB5 SA_DQ_47

DDRA_SDQ49 AY7 SA_DQ_48

DDRA_SDQ50 AT5 SA_DQ_49

DDRA_SDQ51 ATZ SA_DQ_50

DDRA_SDQ52 AY6 SA_DQ_51

DDRA_SDQ53 BB7 SA_DQ_52

DDRA_SDQ54 AR5 SA_DQ_53

DDRA_SDQ55 AR8 SA_DQ_54

DDRA_SDQ56 AR9 SA_DQ_55

DDRA_SDQ57 AN3 SA_DQ_56

DDRA_SDQ58 AM8 SA_DQ_57

DDRA_SDQ59 AN10 SA_DQ_58

DDRA_SDQ60 AT9 SA_DQ_59

DDRA_SDQ61 AN9 SA_DQ_60

DDRA_SDQ62 AM9 SA_DQ_61

DDRA_SDQ63 AN11 SA_DQ_62

DDR SYSTEM MEMORY A

SA_BS_0 BB19 DDRB_SBS0# <14>

SA_BS_1 BK19 DDRB_SBS1# <14>

SA_BS_2 BF29 DDRB_SBS2# <14>

SA_DM_0 AT45 DDRB_SDM0

SA_DM_1 BD44 DDRB_SDM1

SA_DM_2 BD42 DDRB_SDM2

SA_DM_3 AW38 DDRB_SDM3

SA_DM_4 AW13 DDRB_SDM4

SA_DM_5 BG8 DDRB_SDM5

SA_DM_6 AY5 DDRB_SDM6

SA_DM_7 AN6 DDRB_SDM7

SA_DQS_0 AT46 DDRB_SDQS0 DDRB_SDQS0 <14>

SA_DQS_1 BE48 DDRB_SDQS1 DDRB_SDQS1 <14>

SA_DQS_2 BB43 DDRB_SDQS2 DDRB_SDQS2 <14>

SA_DQS_3 BB16 DDRB_SDQS3 DDRB_SDQS3 <14>

SA_DQS_4 BH6 DDRB_SDQS4 DDRB_SDQS4 <14>

SA_DQS_5 BB2 DDRB_SDQS5 DDRB_SDQS5 <14>

SA_DQS_6 AP3 DDRB_SDQS6 DDRB_SDQS6 <14>

SA_DQS_7 AP3 DDRB_SDQS7 DDRB_SDQS7 <14>

SA_DQS#_0 AT47 DDRB_SDQS#0# DDRB_SDQS#0# <14>

SA_DQS#_1 BD47 DDRB_SDQS#1# DDRB_SDQS#1# <14>

SA_DQS#_2 BC41 DDRB_SDQS#2# DDRB_SDQS#2# <14>

SA_DQS#_3 BA37 DDRB_SDQS#3# DDRB_SDQS#3# <14>

SA_DQS#_4 BA16 DDRB_SDQS#4# DDRB_SDQS#4# <14>

SA_DQS#_5 BH7 DDRB_SDQS#5# DDRB_SDQS#5# <14>

SA_DQS#_6 BC1 DDRB_SDQS#6# DDRB_SDQS#6# <14>

SA_DQS#_7 AP2 DDRB_SDQS#7# DDRB_SDQS#7# <14>

SA_MA_0 BJ19 DDRB_SMA0

SA_MA_1 BD20 DDRB_SMA1

SA_MA_2 BK27 DDRB_SMA2

SA_MA_3 BH28 DDRB_SMA3

SA_MA_4 BL24 DDRB_SMA4

SA_MA_5 BK28 DDRB_SMA5

SA_MA_6 BJ27 DDRB_SMA6

SA_MA_7 BJ25 DDRB_SMA7

SA_MA_8 BL28 DDRB_SMA8

SA_MA_9 BC19 DDRB_SMA9

SA_MA_10 BE28 DDRB_SMA10

SA_MA_11 RG30 DDRB_SMA11

SA_MA_12 BJ16 DDRB_SMA12

SA_MA_13 BJ16 DDRB_SMA13

SA_CAS# BL17 DDRB_SCAS# <14>

SA_RAS# BE18 DDRB_SRAS# <14>

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SA_RCVEN# AY20 SA_RCVEN# PAD T4

CRESTLINE ES_FCBGA1299-D
GMR1@

U5E

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DDRB_SDQ1 AR51 SB_DQ_1

DDRB_SDQ2 AW50 SB_DQ_2

DDRB_SDQ3 AW51 SB_DQ_3

DDRB_SDQ4 AN50 SB_DQ_4

DDRB_SDQ5 AN51 SB_DQ_5

DDRB_SDQ6 AV50 SB_DQ_6

DDRB_SDQ7 AV49 SB_DQ_7

DDRB_SDQ8 BA50 SB_DQ_8

DDRB_SDQ9 BB50 SB_DQ_9

DDRB_SDQ10 BA49 SB_DQ_10

DDRB_SDQ11 BE50 SB_DQ_11

DDRB_SDQ12 BE51 SB_DQ_12

DDRB_SDQ13 AY49 SB_DQ_13

DDRB_SDQ14 BE50 SB_DQ_14

DDRB_SDQ15 BF49 SB_DQ_15

DDRB_SDQ16 BJ50 SB_DQ_16

DDRB_SDQ17 BJ44 SB_DQ_17

DDRB_SDQ18 BJ43 SB_DQ_18

DDRB_SDQ19 BL43 SB_DQ_19

DDRB_SDQ20 BK47 SB_DQ_20

DDRB_SDQ21 BK49 SB_DQ_21

DDRB_SDQ22 BK43 SB_DQ_22

DDRB_SDQ23 BK42 SB_DQ_23

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DDRB_SDQ33 BE11 SB_DQ_33

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DDRB_SDQ35 BC11 SB_DQ_35

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DDRB_SDQ37 BE12 SB_DQ_37

DDRB_SDQ38 BC12 SB_DQ_38

DDRB_SDQ39 BG12 SB_DQ_39

DDRB_SDQ40 BJ10 SB_DQ_40

DDRB_SDQ41 BL9 SB_DQ_41

DDRB_SDQ42 BK5 SB_DQ_42

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DDRB_SDQ45 BK10 SB_DQ_45

DDRB_SDQ46 BJ8 SB_DQ_46

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DDRB_SDQ50 BK1 SB_DQ_50

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DDRB_SDQ56 BA3 SB_DQ_56

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DDRB_SDQ58 AR1 SB_DQ_58

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DDRB_SDQ60 AY2 SB_DQ_60

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DDRB_SDQ63 AT2 SB_DQ_63

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SB_DM_4 BH12 DDRB_SDM4

SB_DM_5 BJ7 DDRB_SDM5

SB_DM_6 BE3 DDRB_SDM6

SB_DM_7 AW2 DDRB_SDM7

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SB_MA_5 BE25 DDRB_SMA5

SB_MA_6 BA29 DDRB_SMA6

SB_MA_7 BC28 DDRB_SMA7

SB_MA_8 AY28 DDRB_SMA8

SB_MA_9 DG37 DDRB_SMA9

SB_MA_10 BG17 DDRB_SMA10

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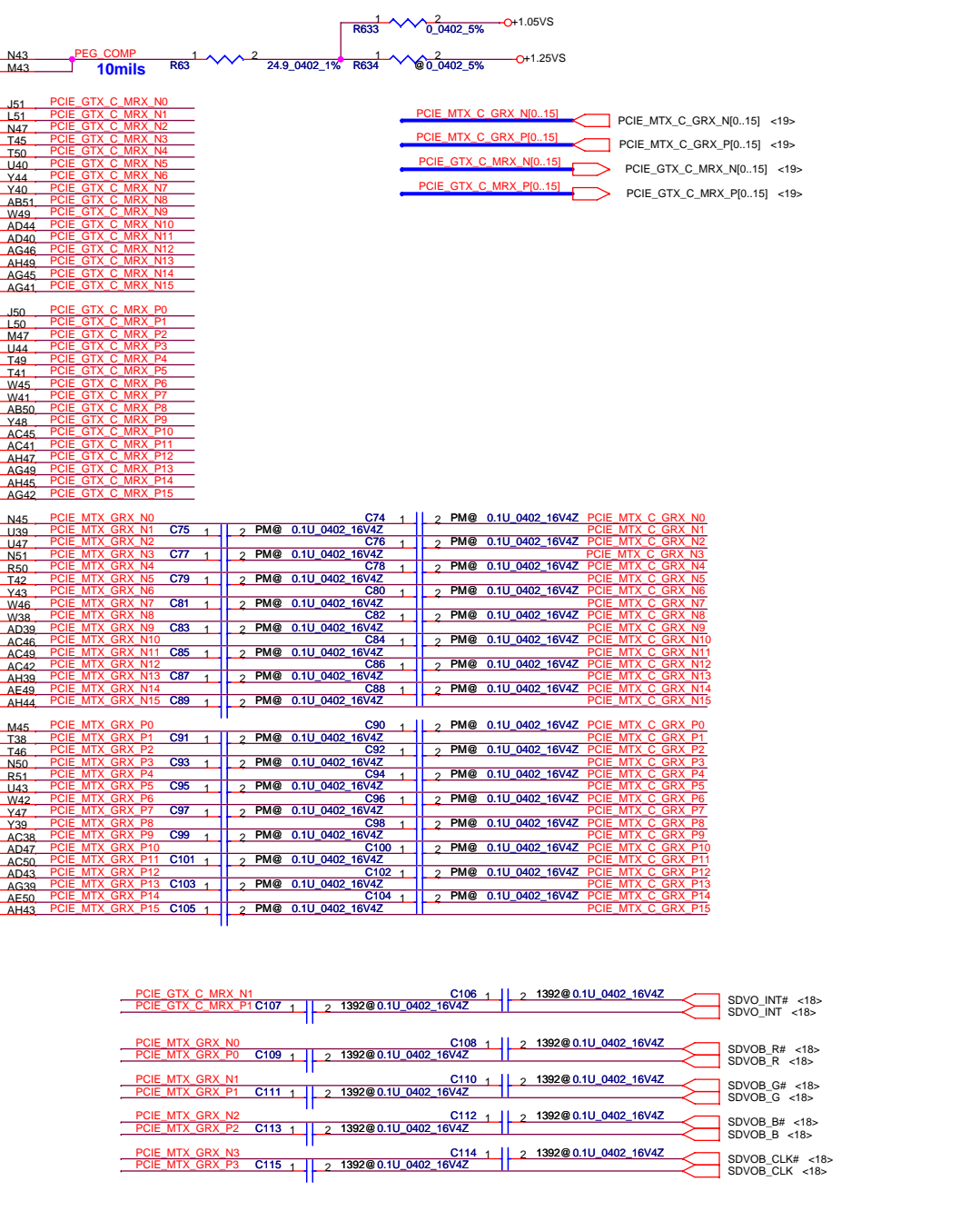
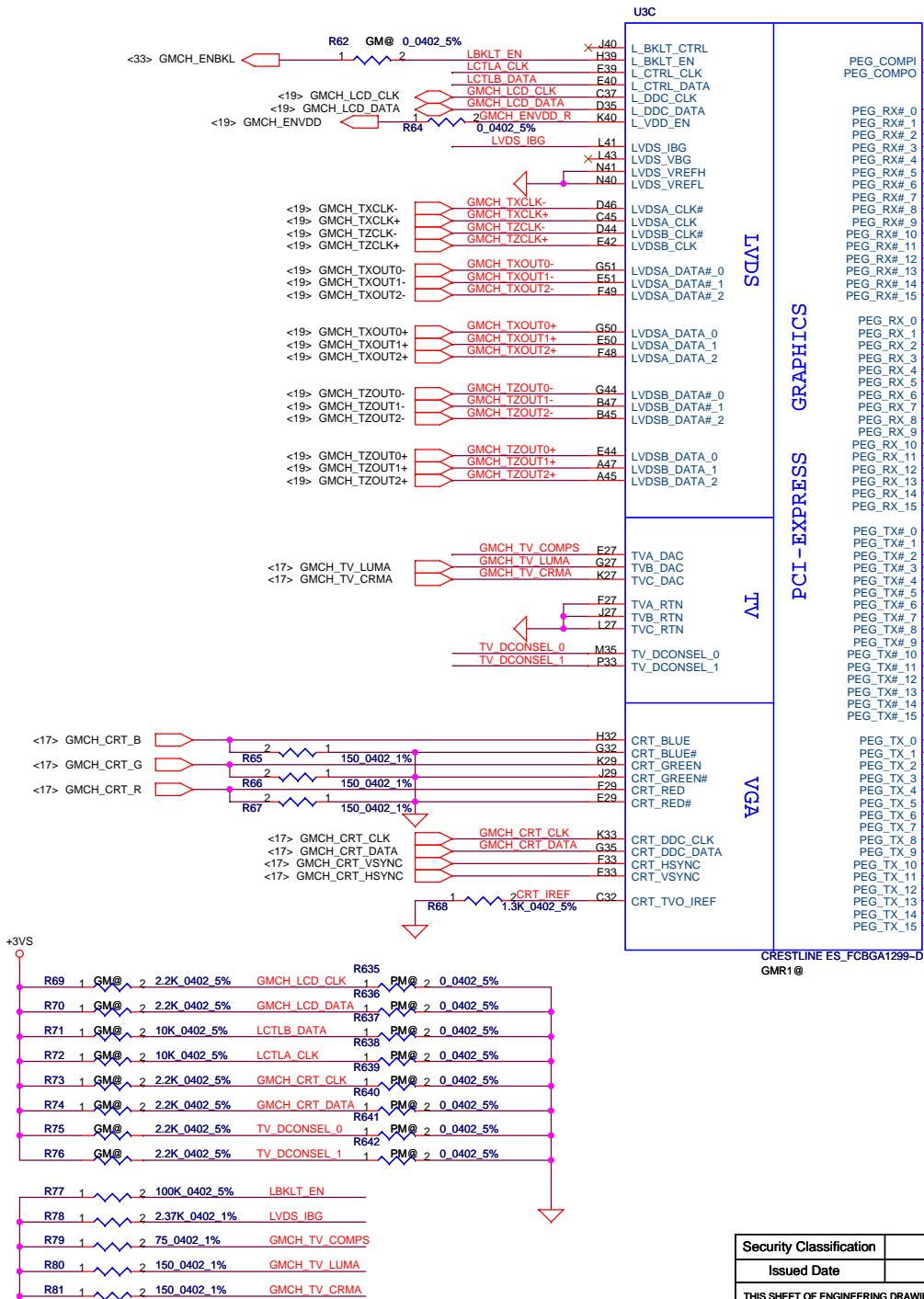
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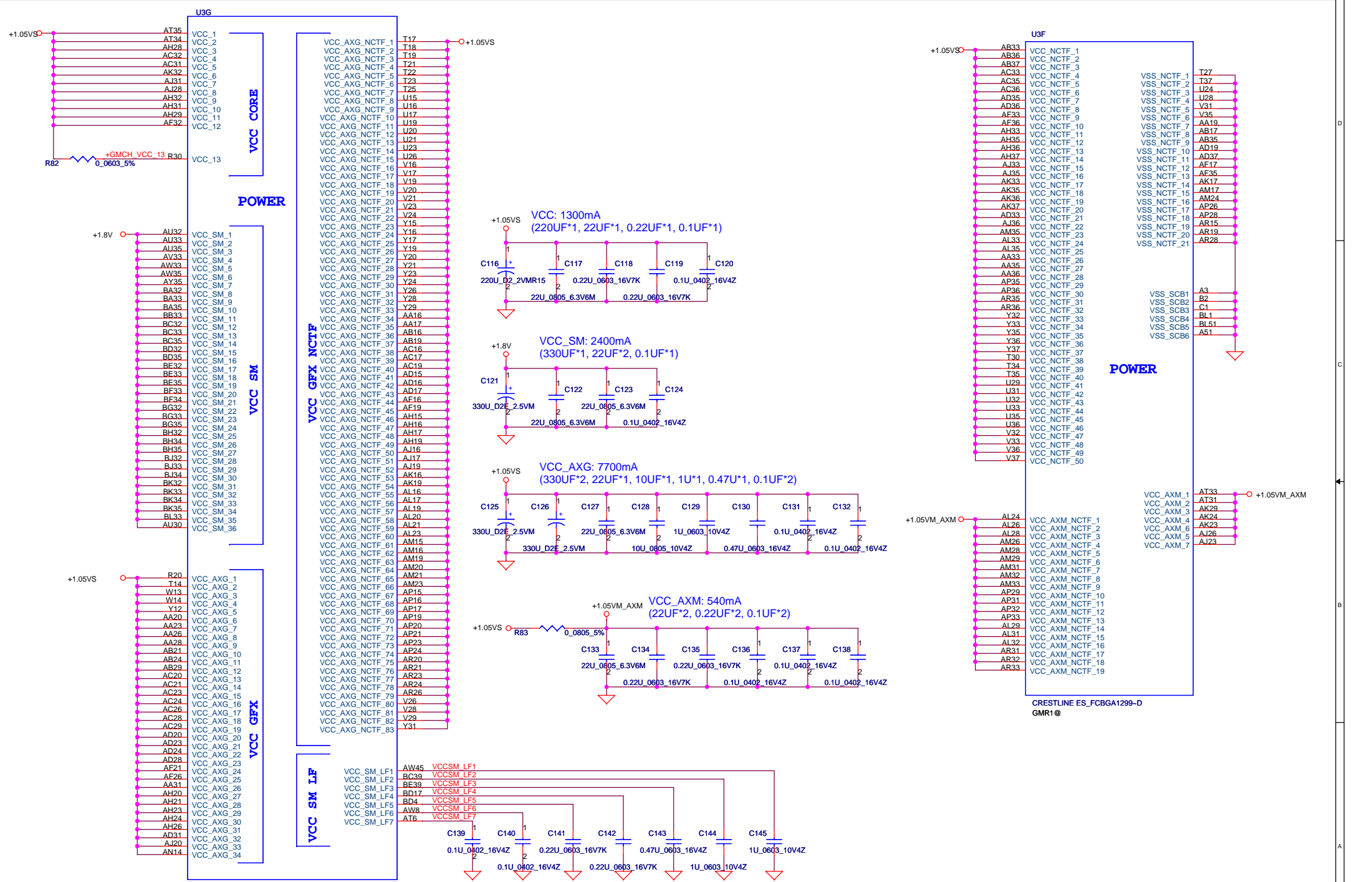
CRESTLINE ES_FCBGA1299-D
GMR1@

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Date:	Friday, September 22, 2006	Sheet	9	of	48



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Size	Document Number	Rev		Date	
B	ISRAA LA-3441P	0.1		Friday, September 22, 2006	
		Sheet	10	of 48	

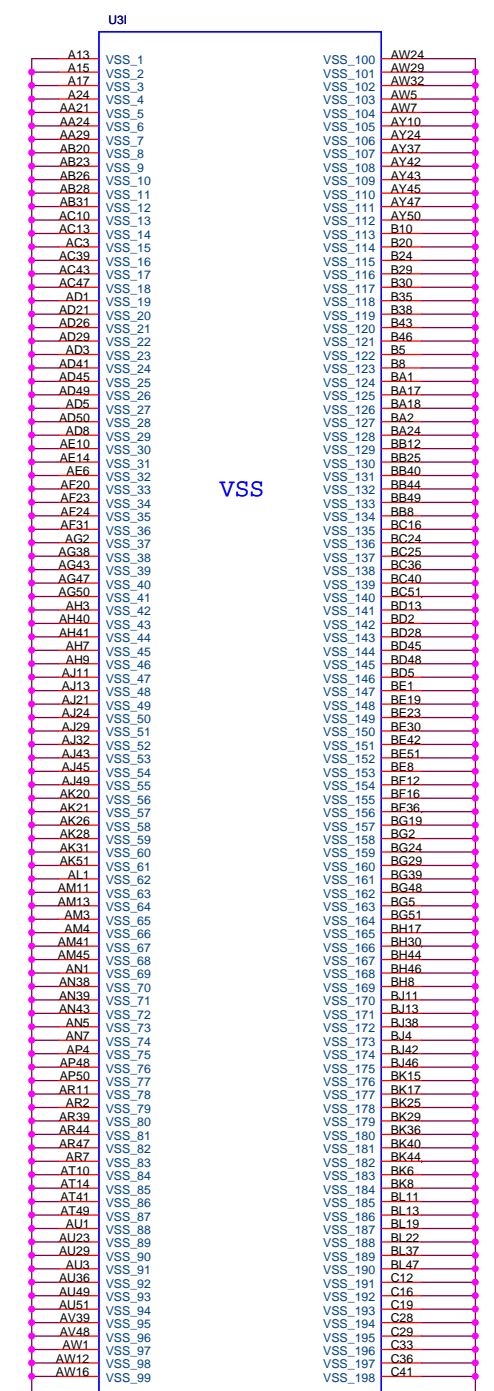
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Crestline(4/7)
ISRAA LA-3441P
 Friday, September 22, 2006 Sheet 10 of 48



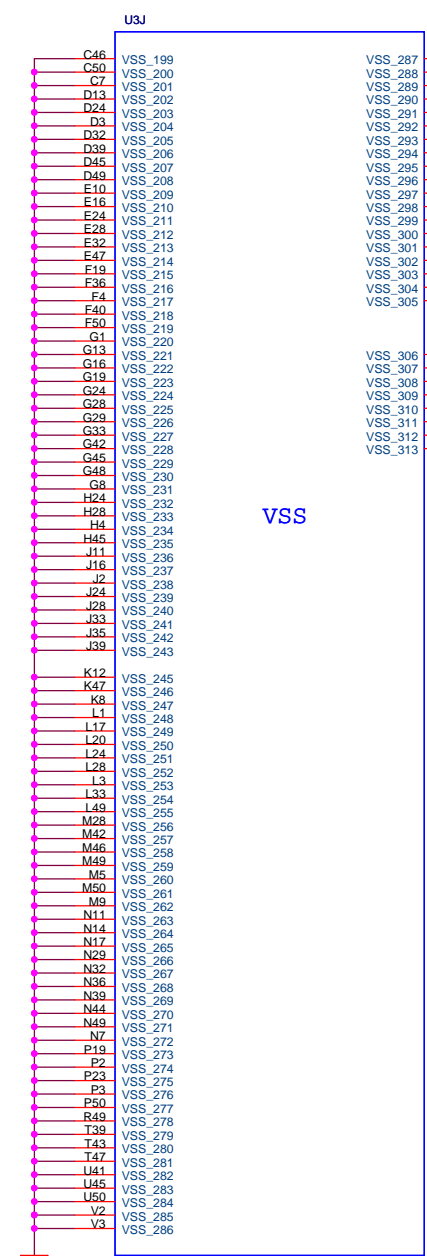
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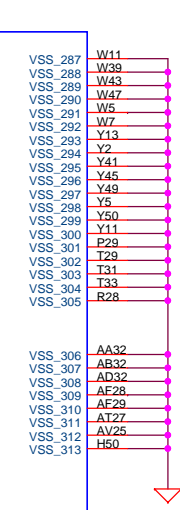
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Title Crestline (5/7)			
Size B	Document Number ISRAA LA-3441P	Rev 0.1	
Date:	Thursday, September 21, 2006	Sheet	11 of 48



CRESTLINE ES_FCBGA1299-D
GMR1@

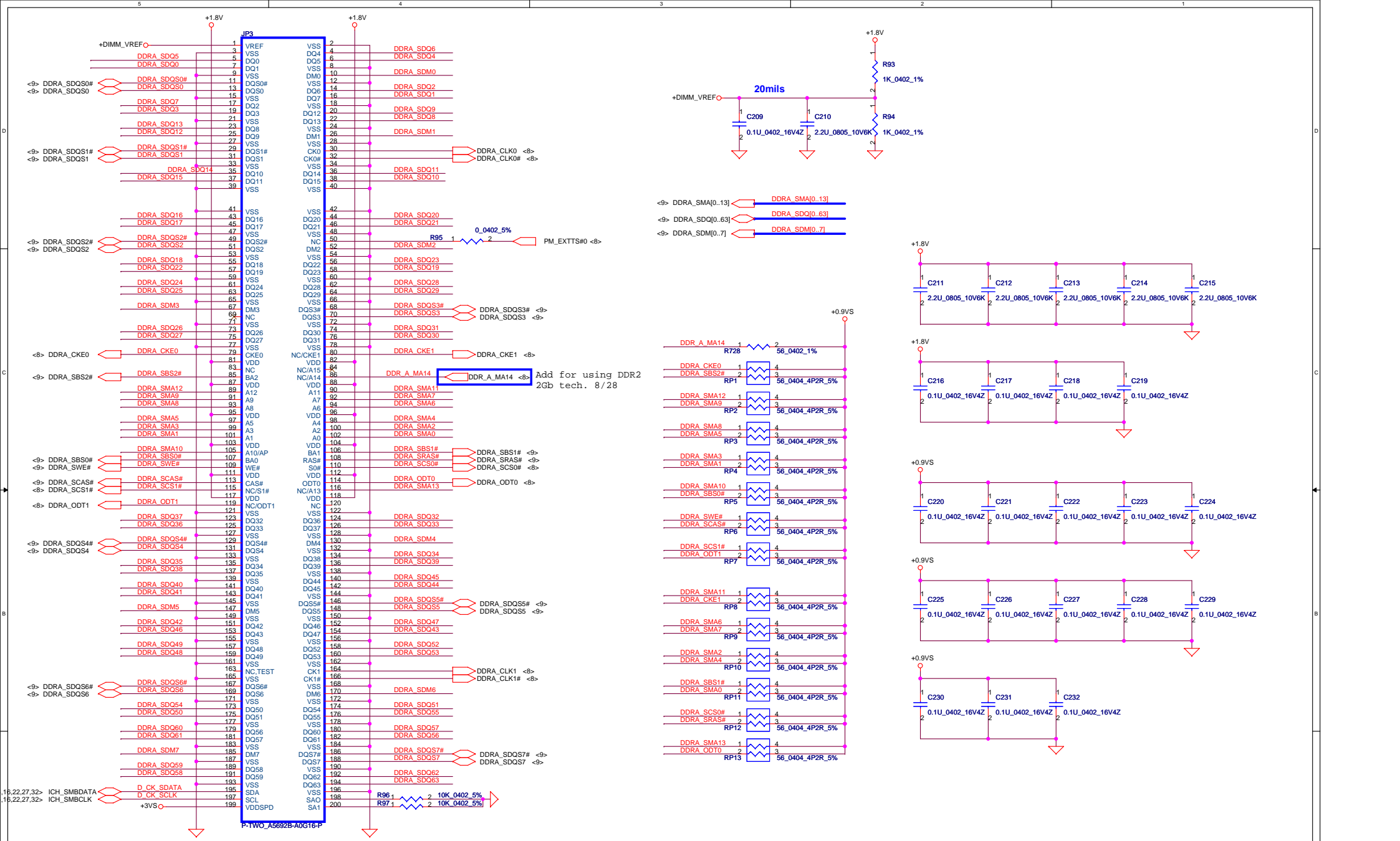


CRESTLINE ES_FCBGA1299-D
GMR1@



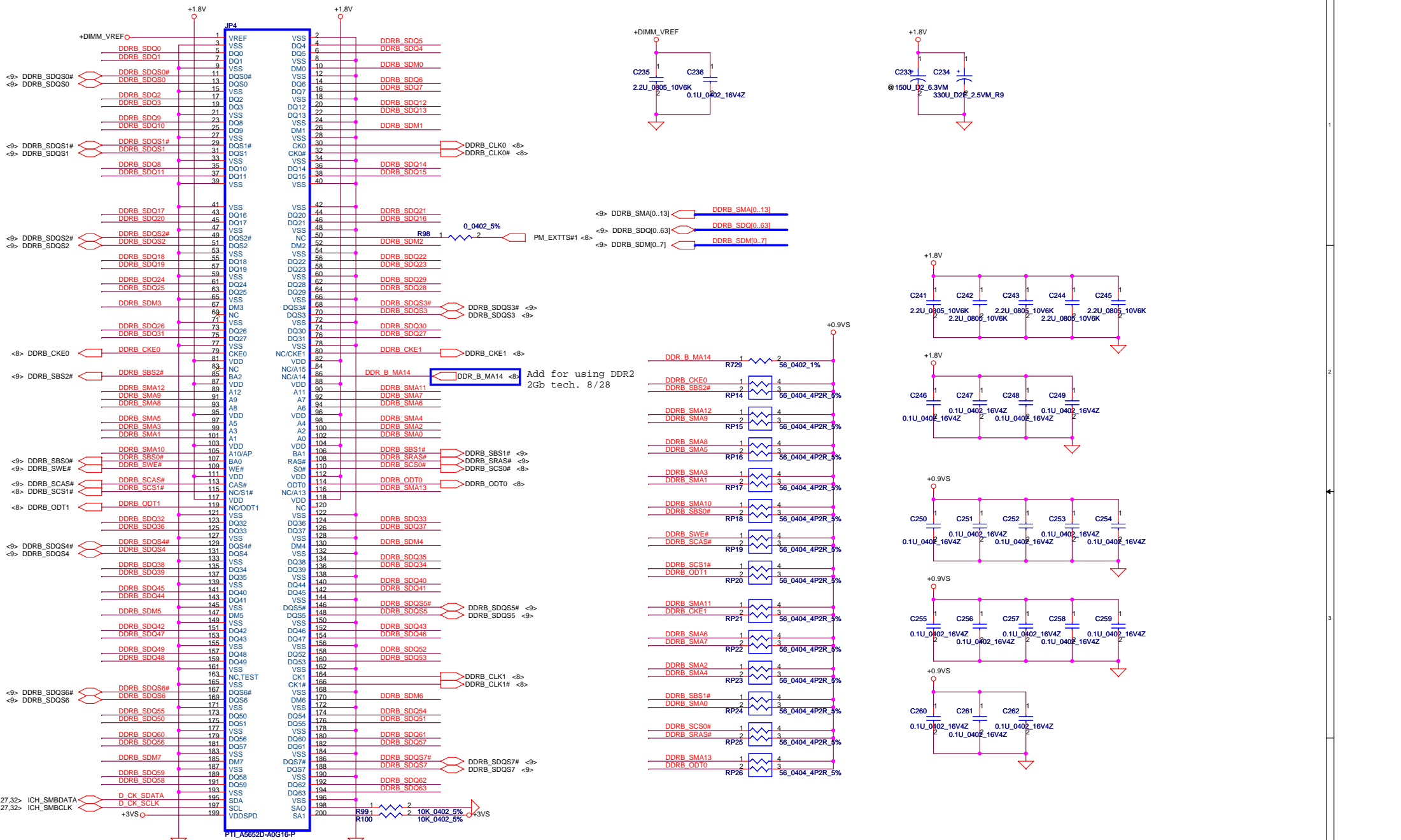
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Date:				Thursday, September 21, 2006	Sheet 13 of 48
				Rev	0.1



DIMM0 STD H:9.2mm (BOT)

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				DDRII-SODIMMO	
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				Date: Friday, September 22, 2006	Rev 0.1
				Sheet 14	of 48



DIMM1 STD H:5.2mm (BOT)

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				Date:	Friday, September 22, 2006
				Sheet	15 of 48

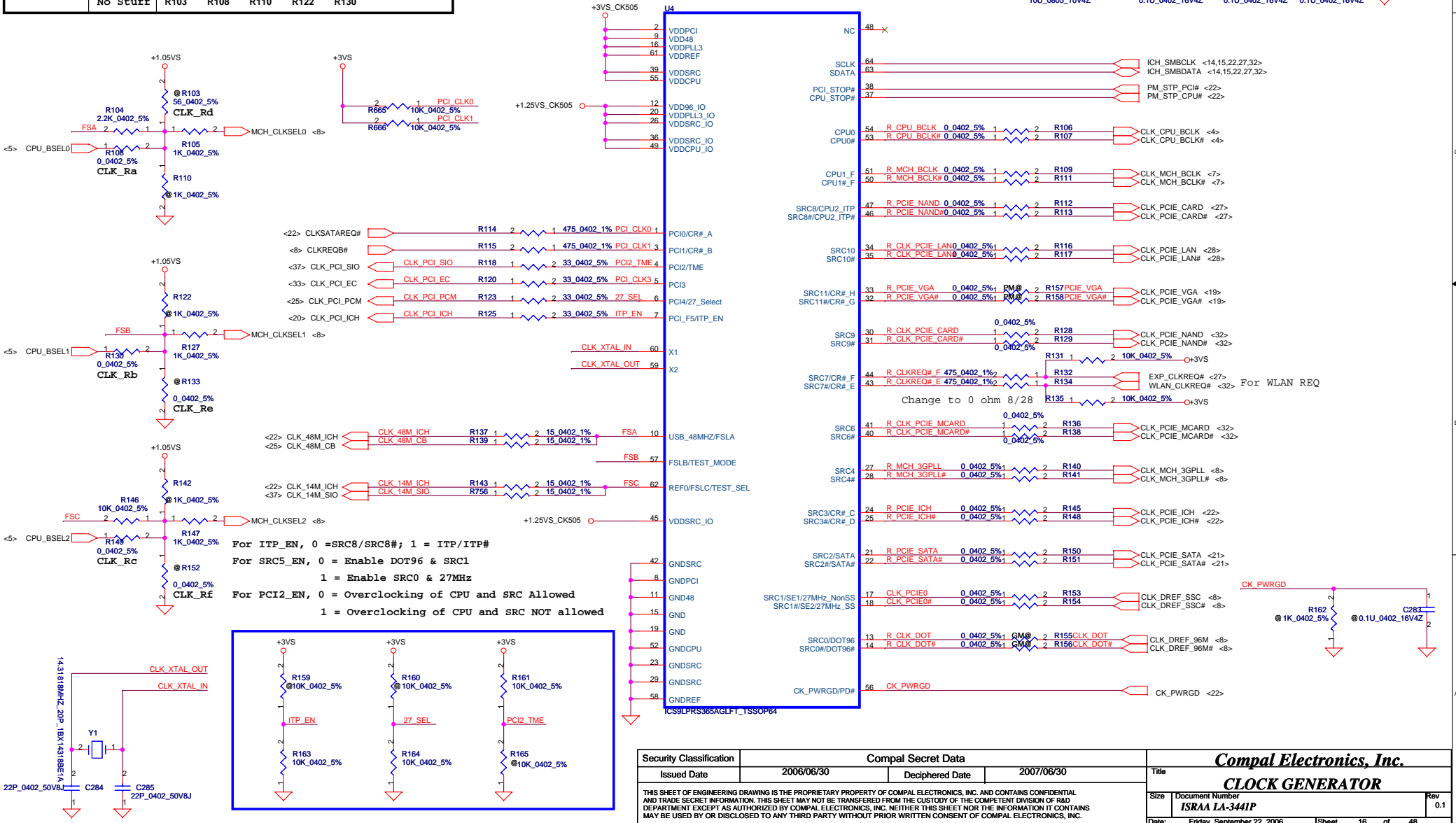
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0	1	1	166	100	33.3

FSB Frequency Select:

CPU Driven	Stuff	R108	R130	R149	R152
* (Default)	No Stuff	R103	R110	R122	R152
667MHz	Stuff	R103	R110	R149	R152
	No Stuff	R108	R122	R130	
800MHz	Stuff			R149	R152
	No Stuff	R103	R108	R110	R122

C263	2	1	CLK_48M_ICH	@5P_0402_50V8C
C264	2	1	CLK_14M_ICH	@4.7P_0402_50V8C
C265	2	1	CLK_PCI_ICH	@4.7P_0402_50V8C
C267	2	1	CLK_PCI_EC	@4.7P_0402_50V8C
C275	2	1	CLK_PCI_PCM	@4.7P_0402_50V8C
C276	2	1	CLK_PCI_SIO	@4.7P_0402_50V8C
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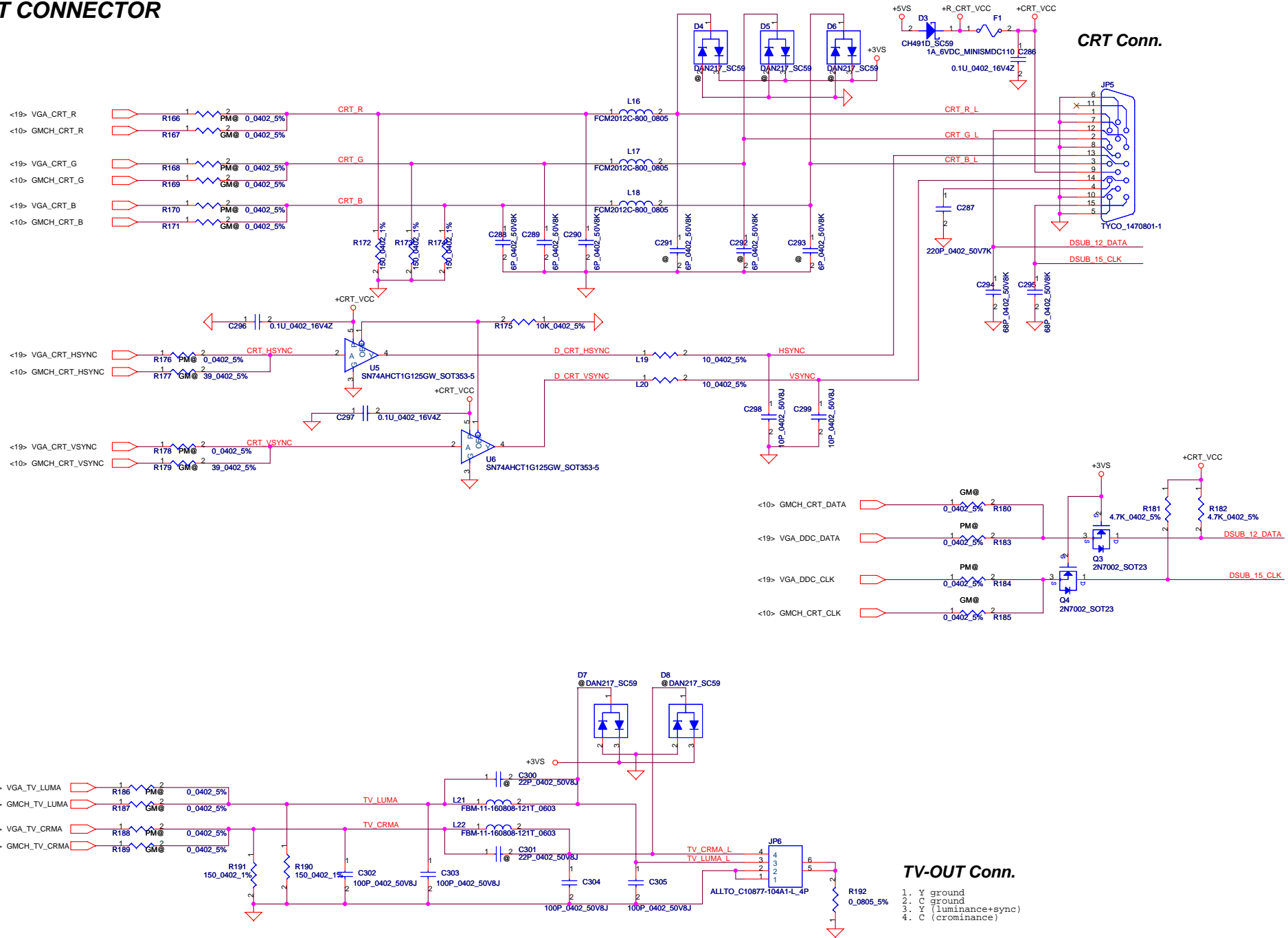
Place close to U4



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CLOCK GENERATOR				
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			ISRAA LA-3441P	0.1
Date:	Friday, September 22, 2006	Sheet	16	of 48

CRT CONNECTOR

Near to JP5

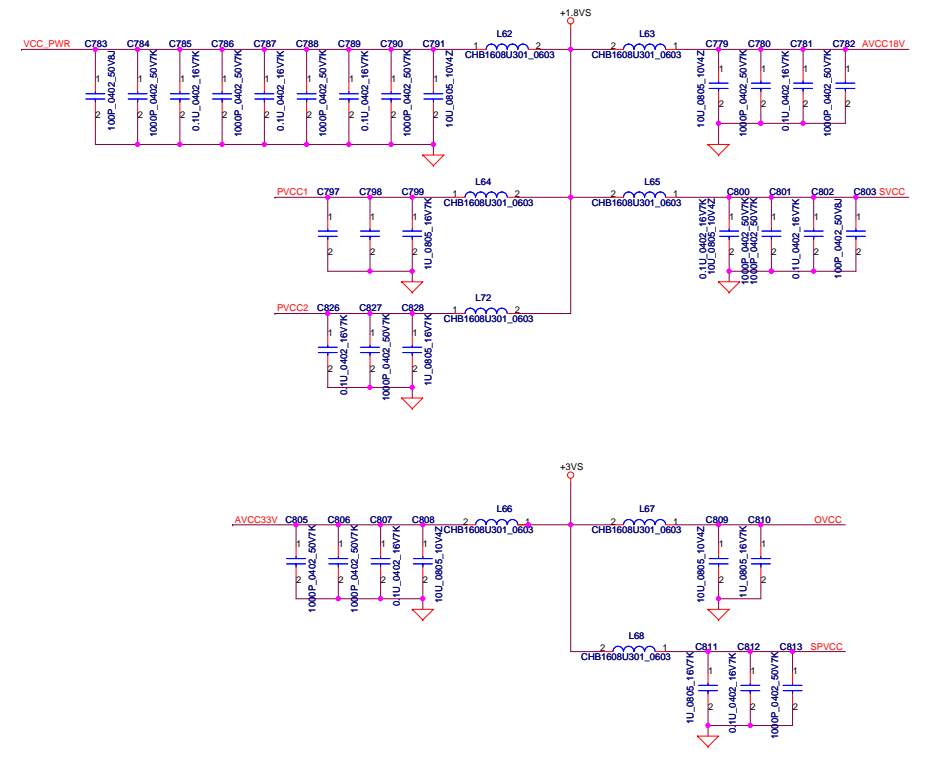
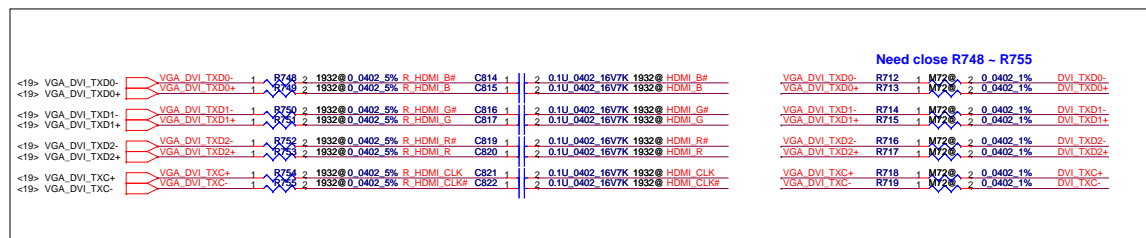
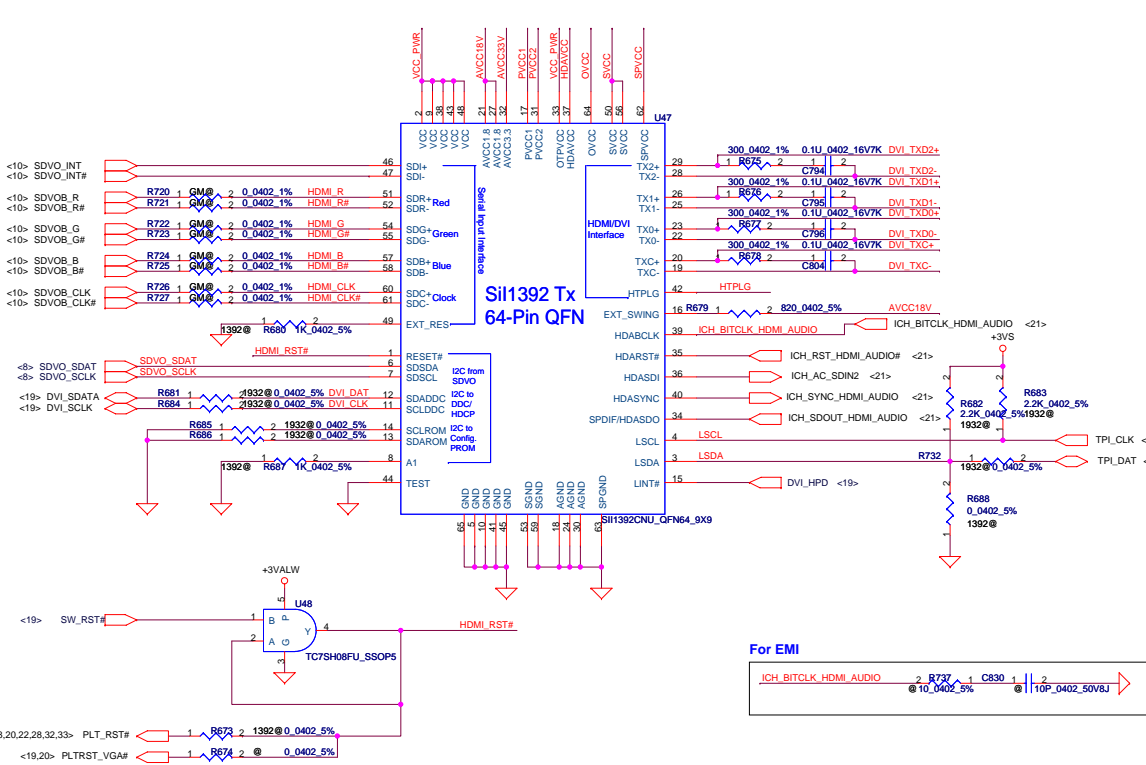


CRT Conn.

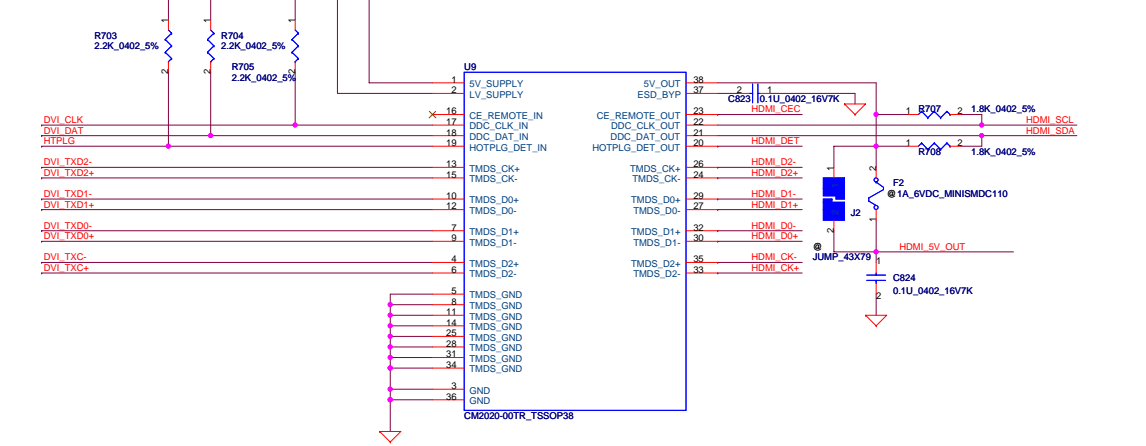
TV-OUT Conn.

- 1. Y ground
- 2. C ground
- 3. Y (luminance+sync)
- 4. C (chrominance)

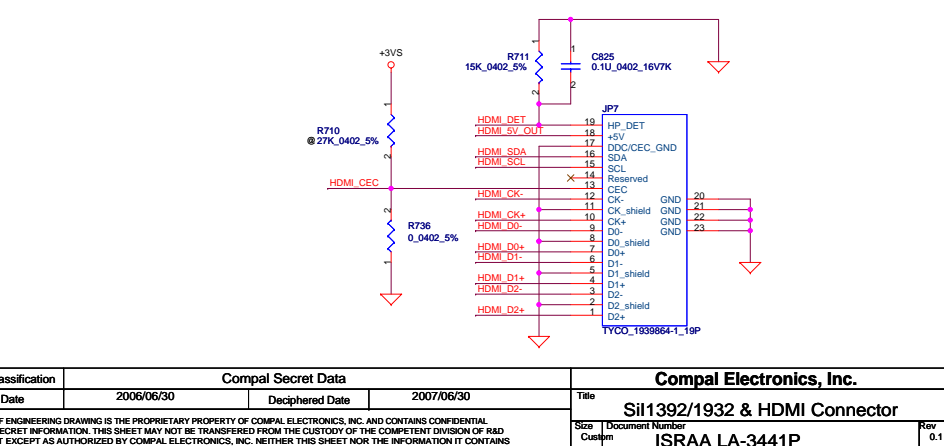
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Issued Date	2006/06/30	Deciphered Date	2007/06/30	CRT & TVout Connector	
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				ISRAA LA-3441P	
				Date:	Friday, September 22, 2006
				Sheet	17 of 48



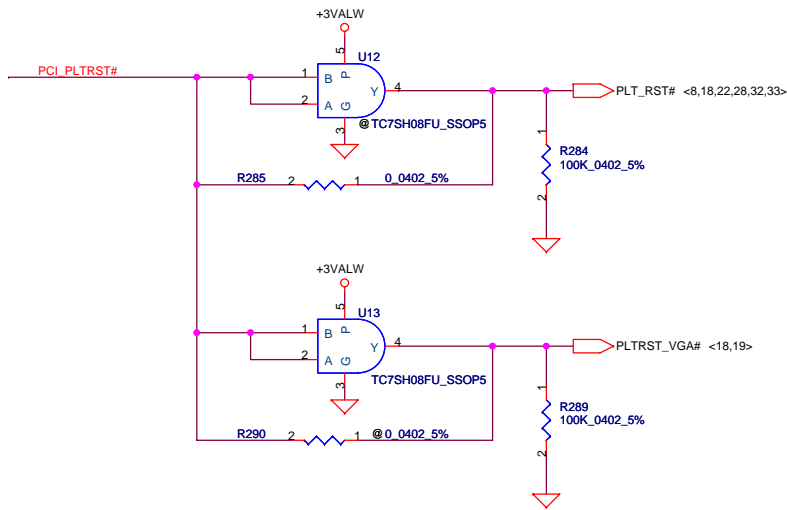
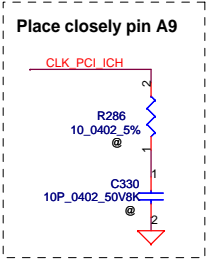
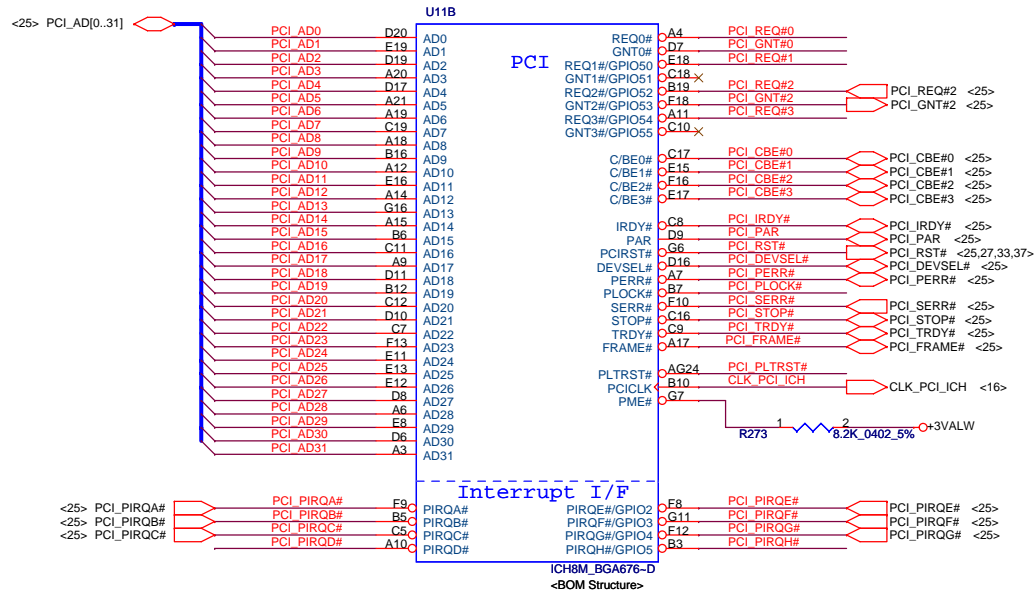
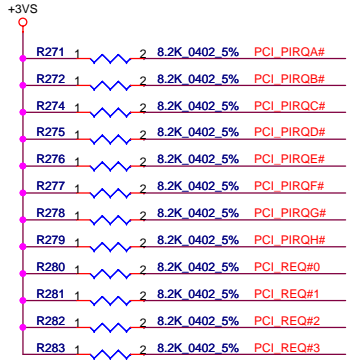
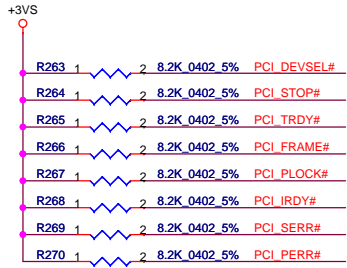
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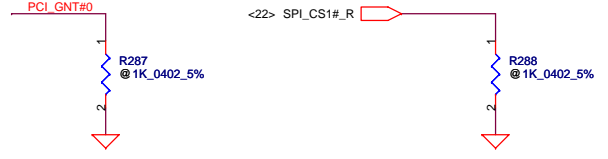
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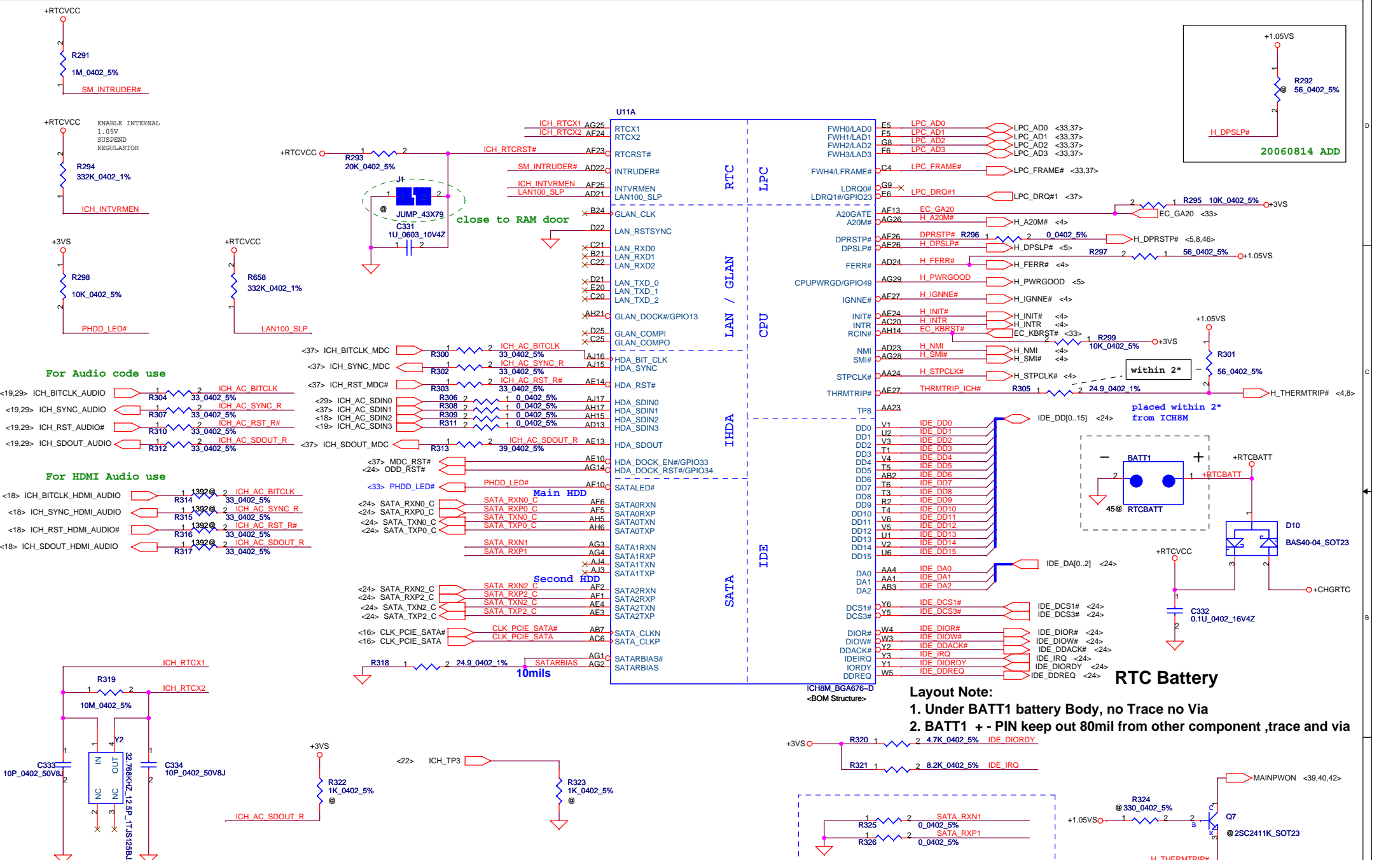


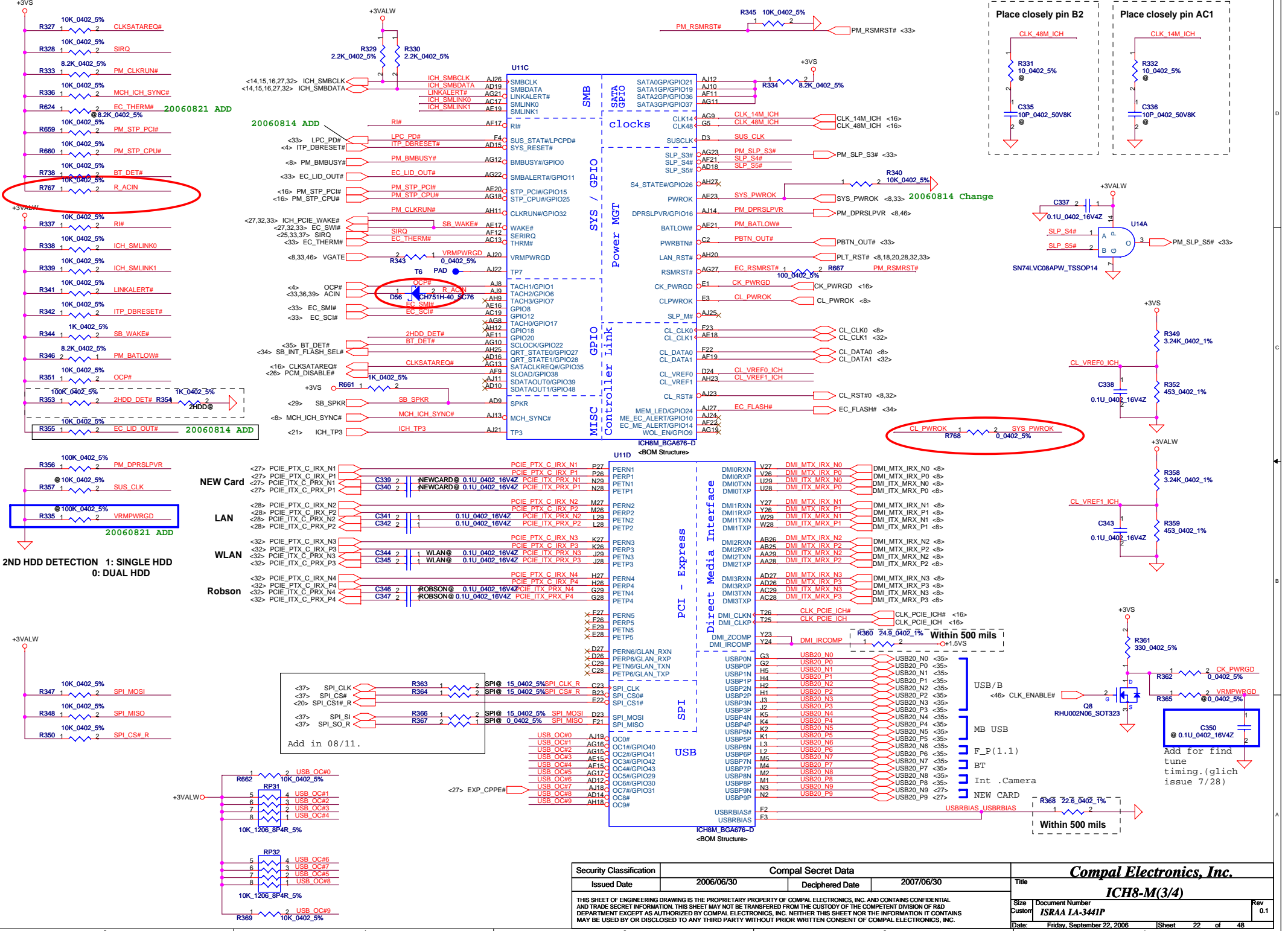
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PCI_GNT0#	SPI_CS#0	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





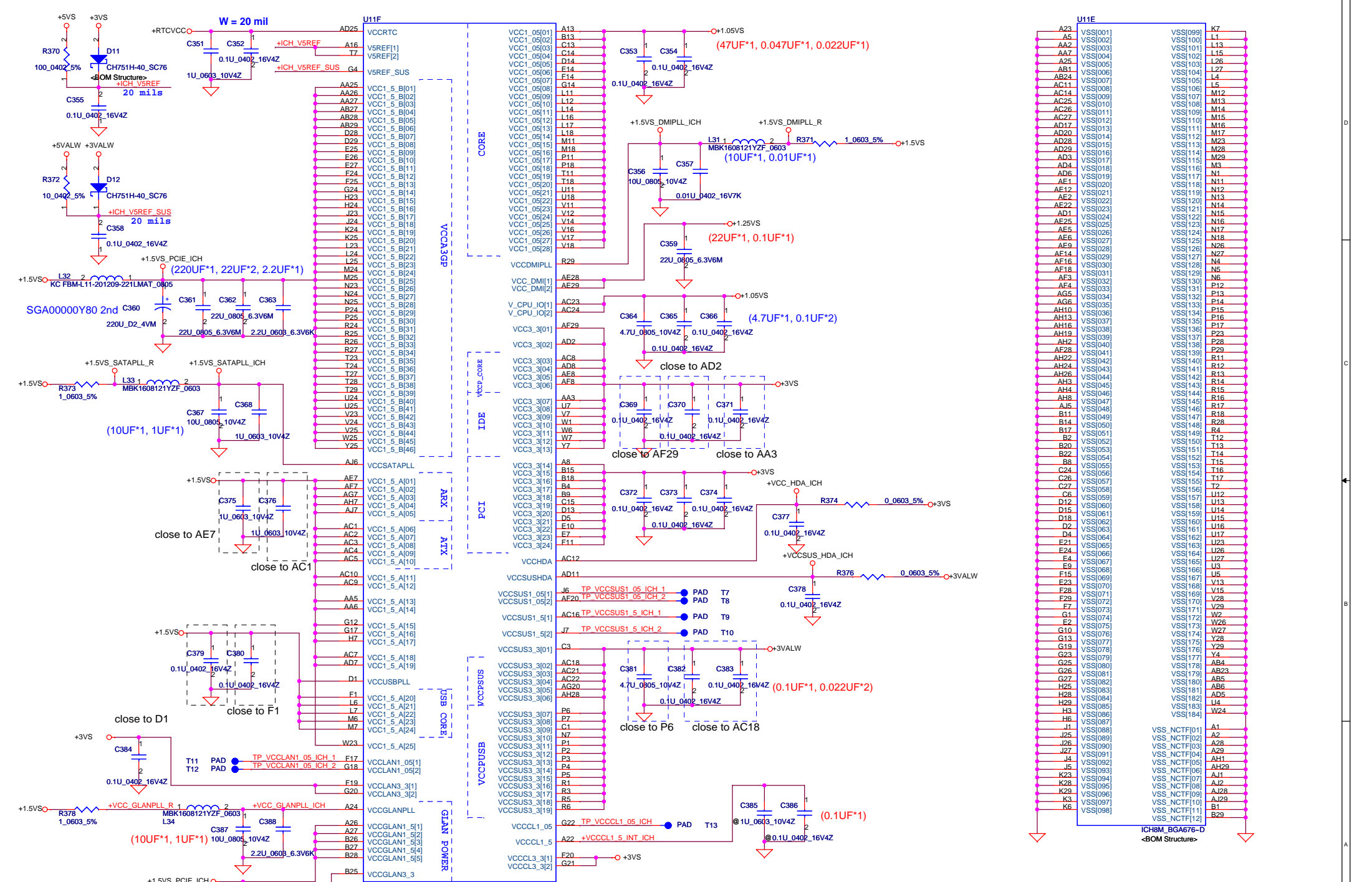


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Add for find tune timing. (gliche issue 7/28)

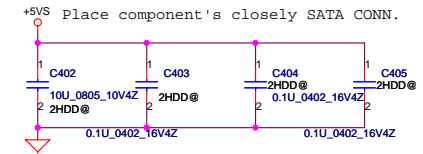
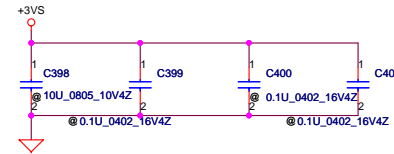
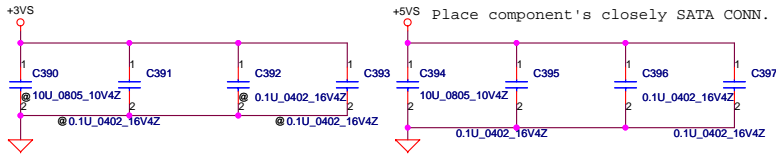


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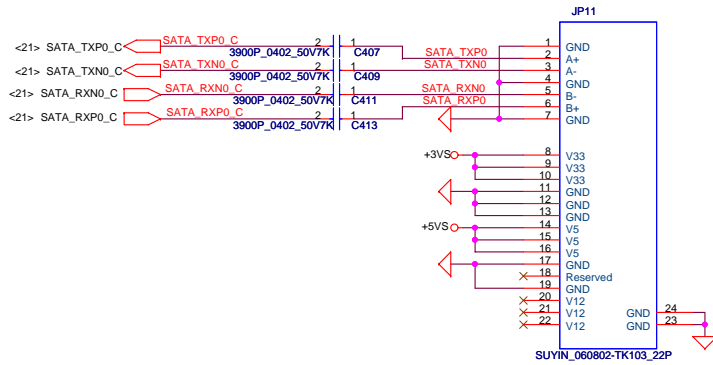
Compal Electronics, Inc.

ICH8-M(4/4)

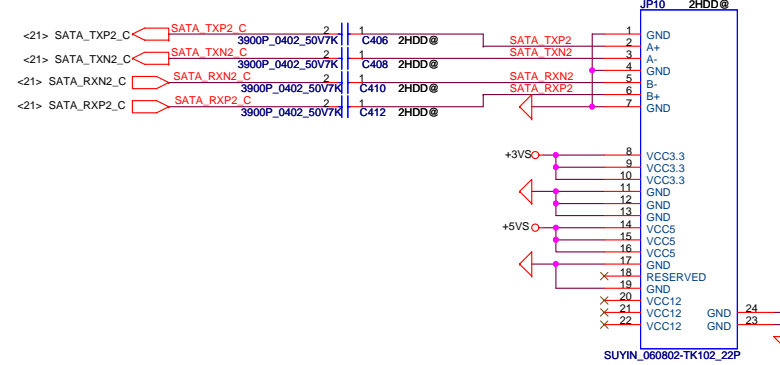
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Date:	Friday, September 22, 2006	Sheet 23 of 48



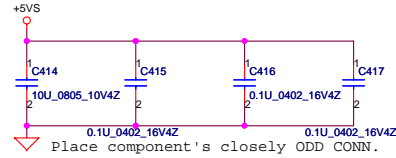
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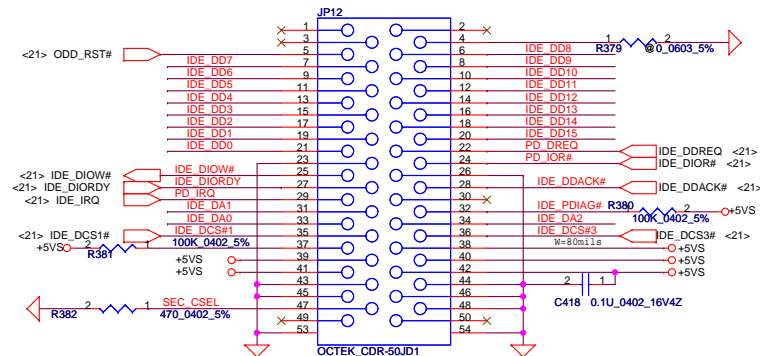
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Place caps. near ODD CONN.

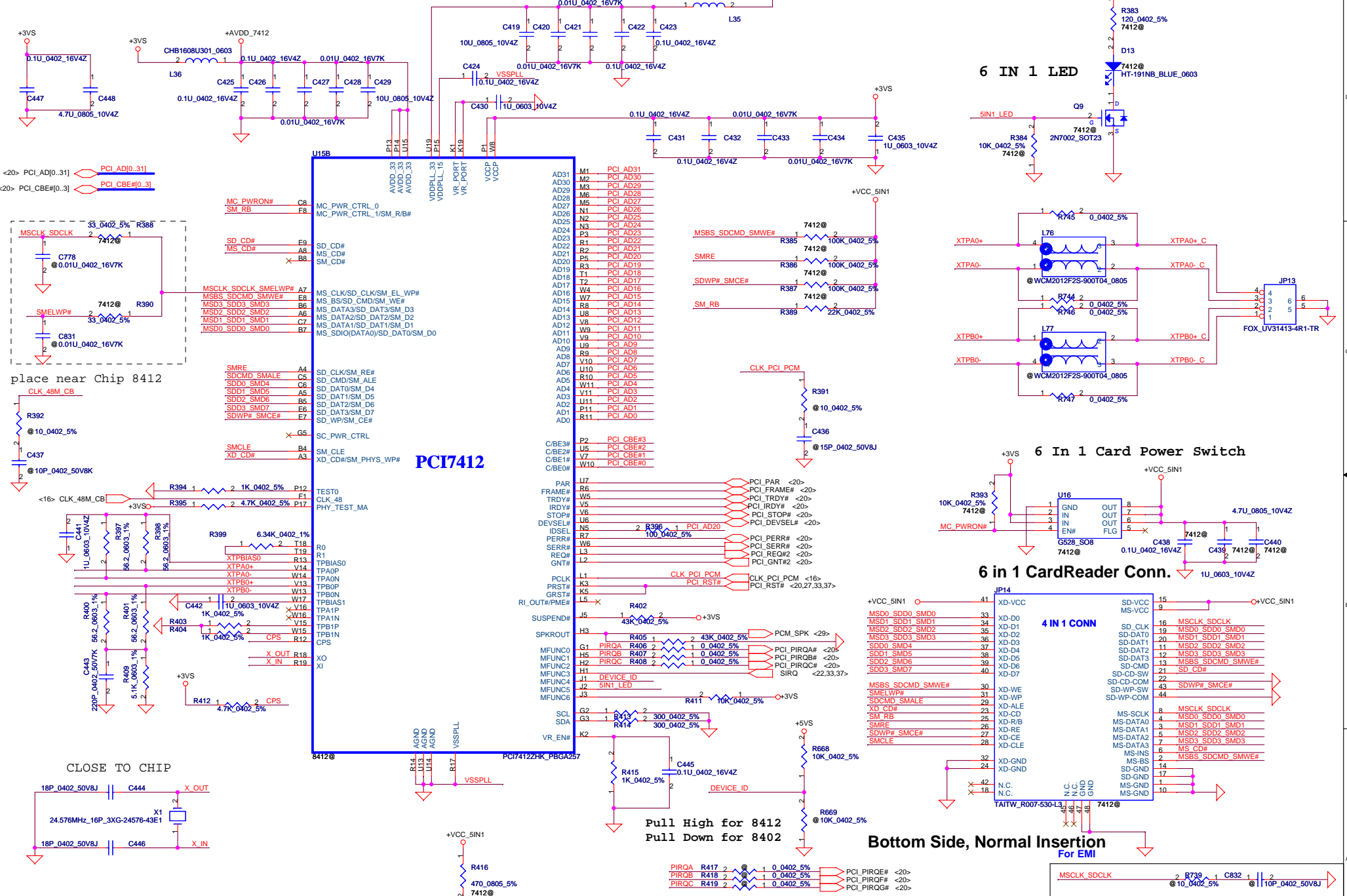


ODD CONN



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Issued Date	2006/06/30	Deciphered Date	2007/06/30	Title		
				SATA & ODD Conn		
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				ISRAA LA-3441P		
				Date:	Friday, September 22, 2006	Sheet 24 of 48

PCI8412:6IN1 + 1394 + CardBus



PCI7412

Pull High for 8412
Pull Down for 8402

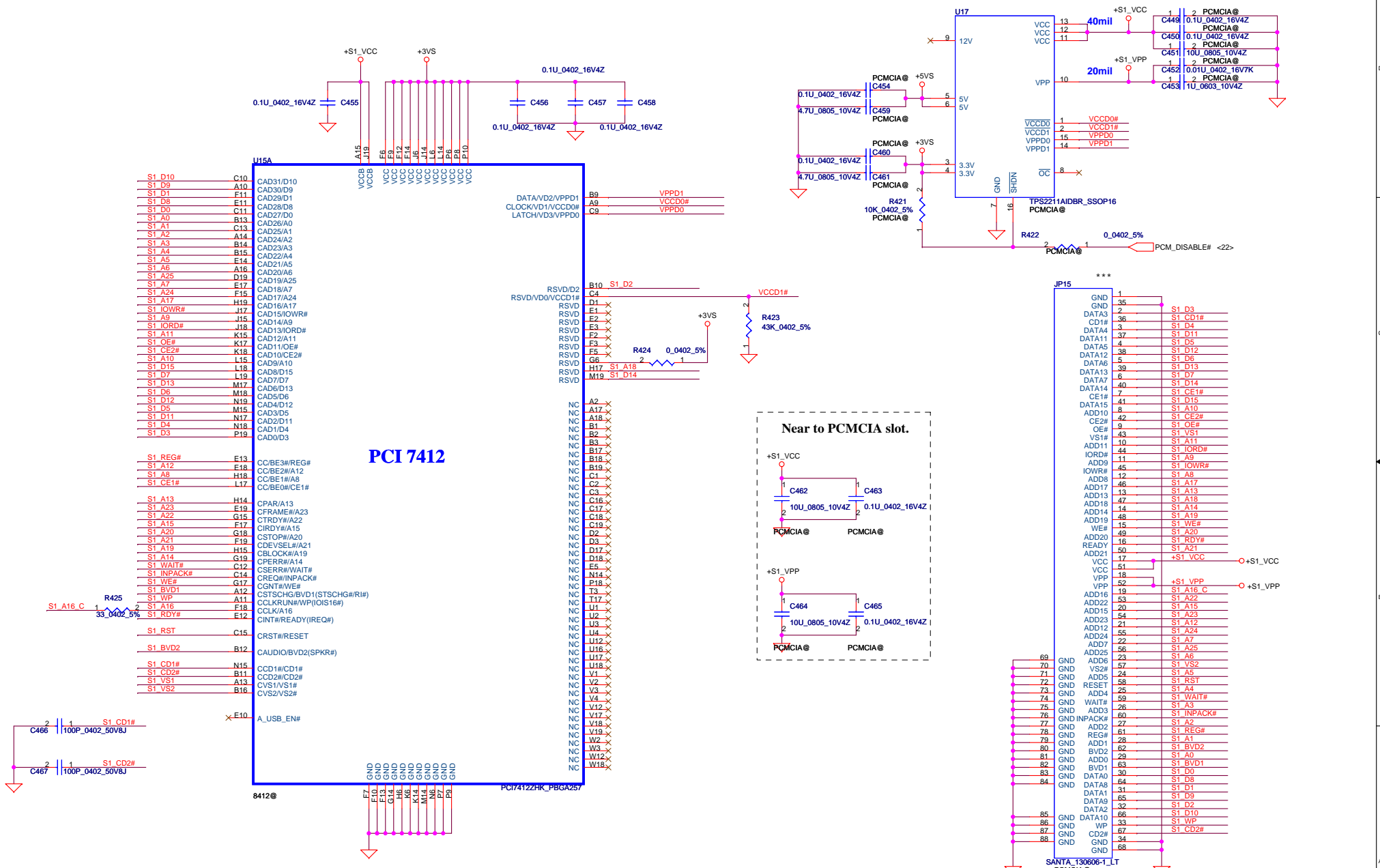
Bottom Side, Normal Insertion
For EMI

Security Classification	Compal Secret Data
Issued Date	2006/06/30
Deciphered Date	2007/06/30

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Compal Electronics, Inc.	
Title PCI8412/PCI1394 CONN/CARD SLOT	
Size Custom	Document Number ISRAA LA-3441P
Date: Friday, September 22, 2006	Rev 0.1
Sheet 25	of 48

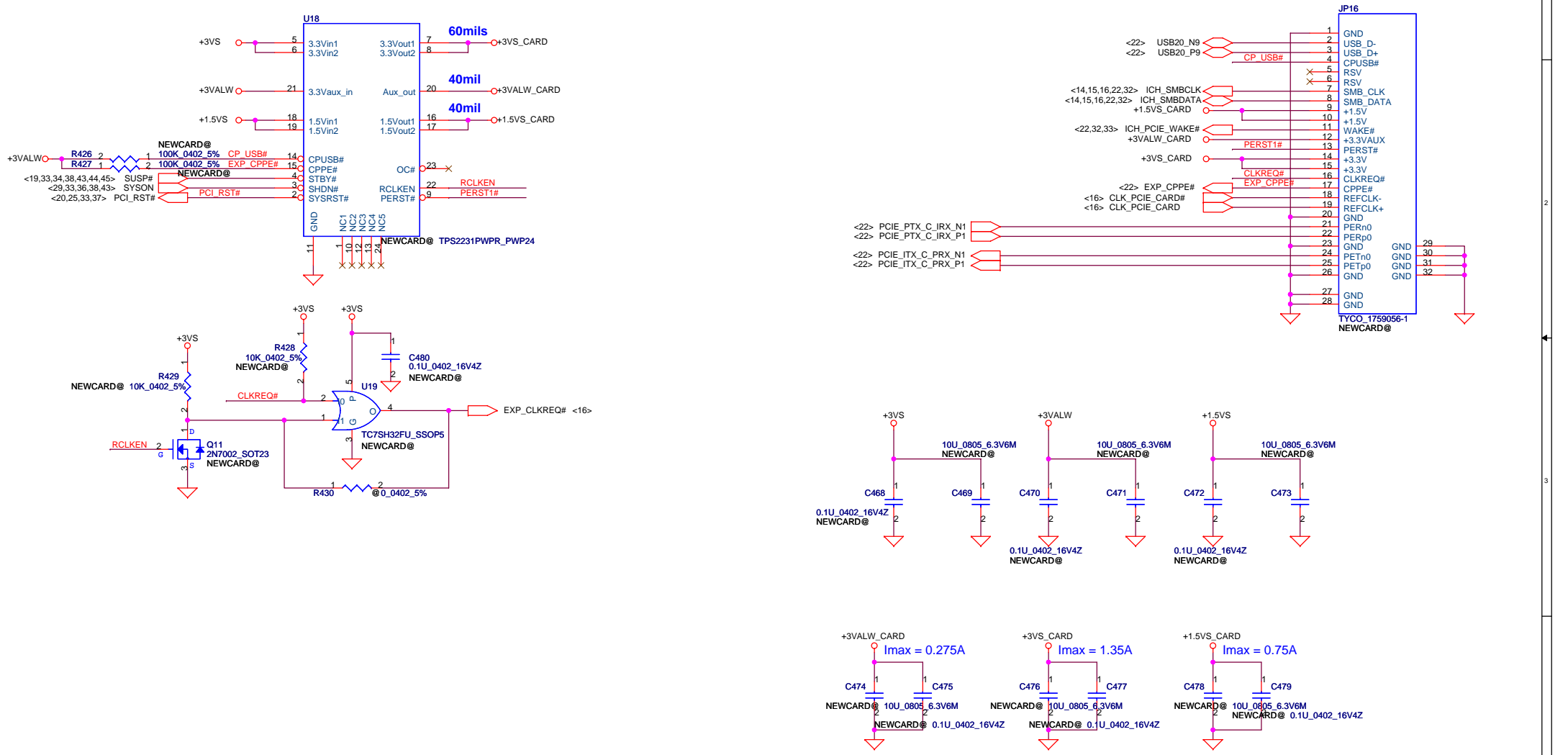
CardBus Power Switch



Security Classification	Compal Secret Data	
Issued Date	2006/06/30	Deciphered Date
		2007/06/30
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Title		Compal Electronics, Inc.	
PCI7412/CB/CB SLOT		Size	Document Number
Customer	ISRAA LA-3441P	Rev	0.1
Date:	Friday, September 22, 2006	Sheet	26 of 48

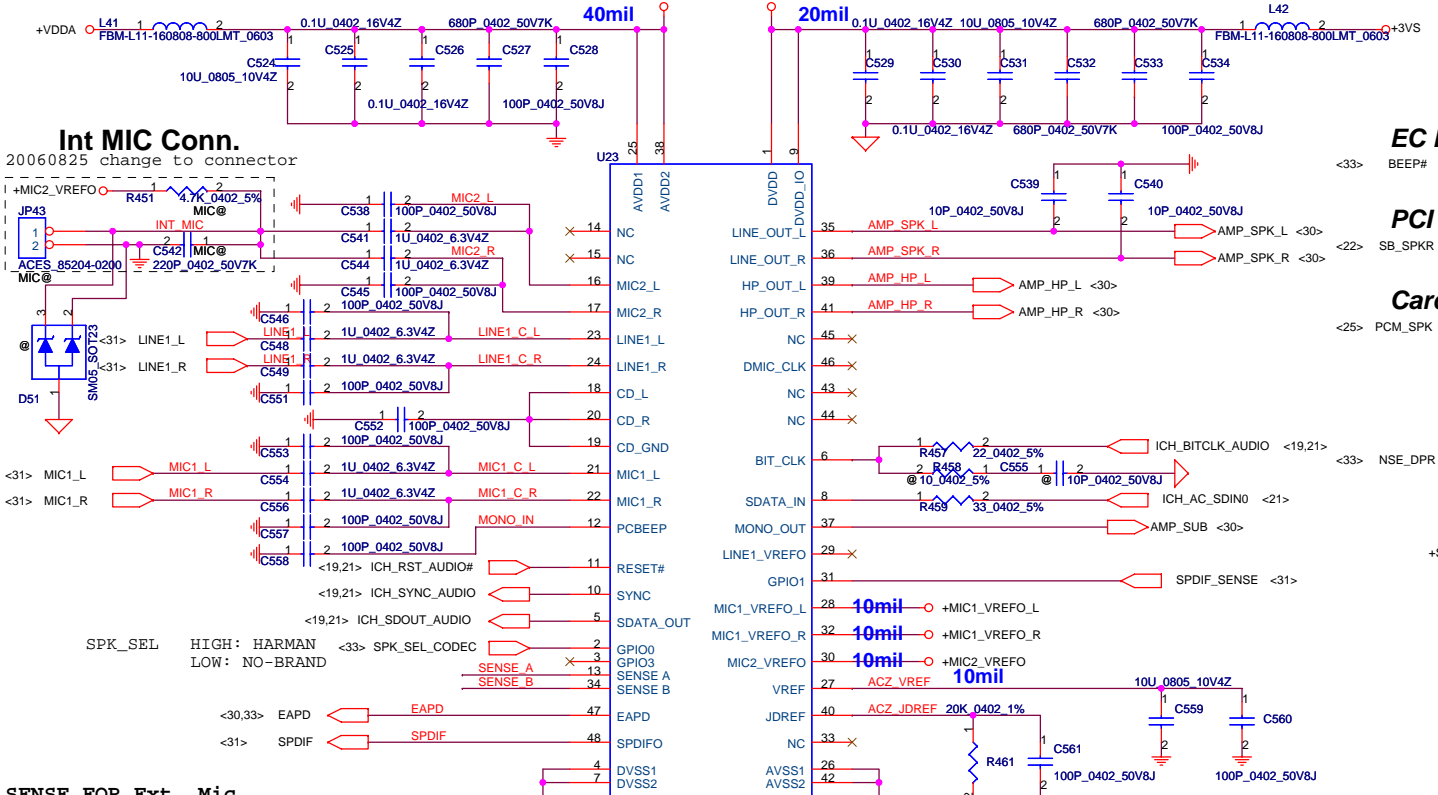
New Card Power Switch



Compal Electronics, Inc.		
Title New Card Socket		
Size	Document Number ISRAA LA-3441P	Rev 0.1
Date:	Friday, September 22, 2006	Sheet 27 of 48

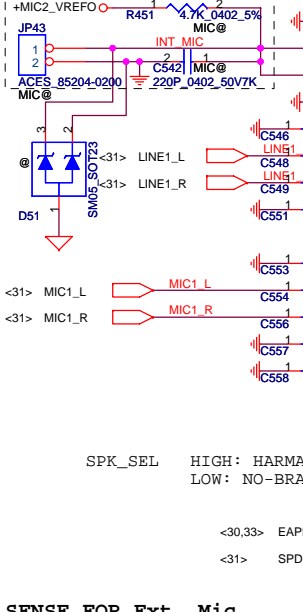
HD Audio Codec

+AVDD_AC97 +3VS_DVDD



Int MIC Conn.

20060825 change to connector



EC BEEP

BEEP#



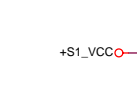
PCI BEEP

SB_SPKR



CardBus BEEP

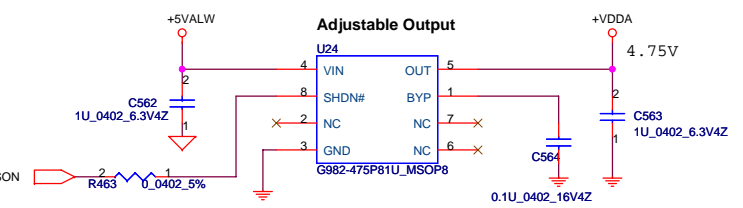
PCM_SPK



NSE DPR



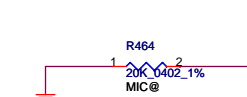
Regulator for CODEC



SENSE FOR Ext. Mic.



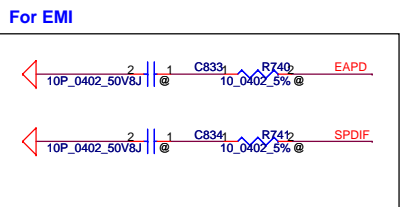
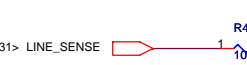
SENSE FOR Int. Mic.



SENSE FOR HP

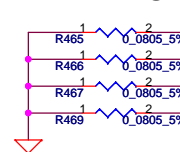


SENSE FOR LINE



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

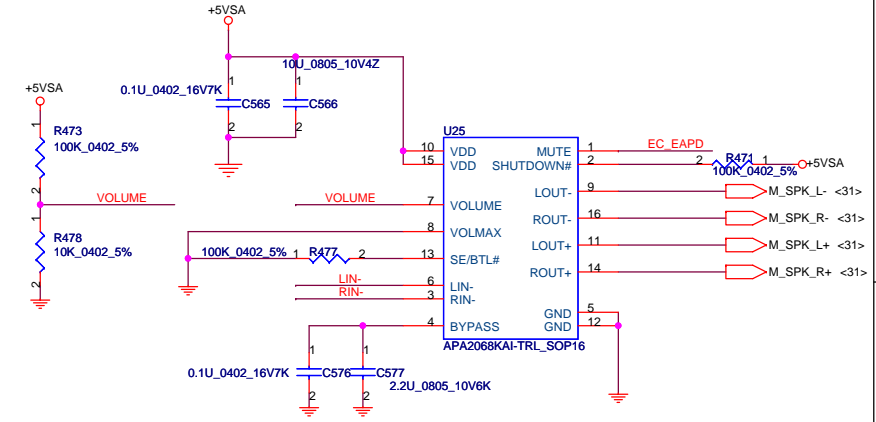
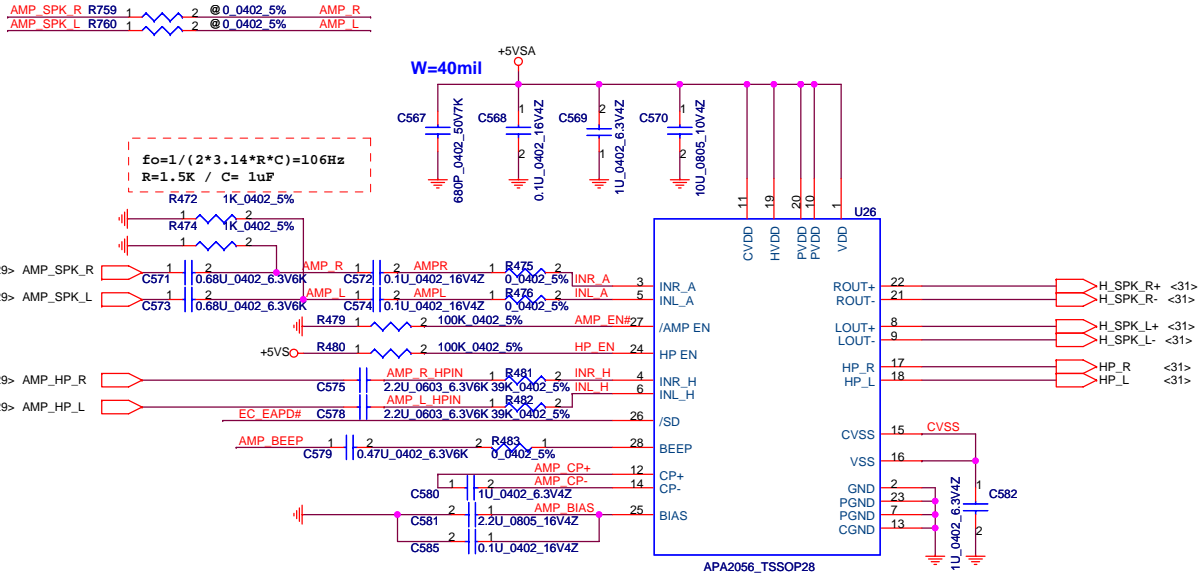
Moat Bridge



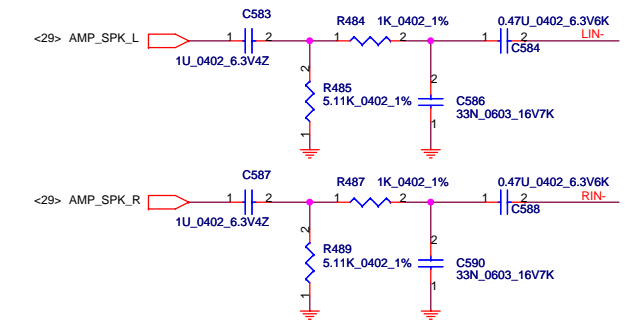
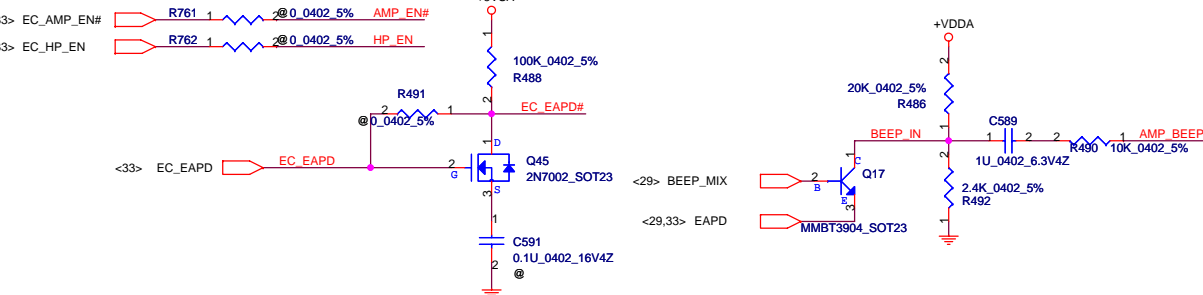
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/06/30	Deciphered Date	2007/06/30	Title
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APA2056 Tweeter/HP Amplifier

APA2068 Medium Range Amplifier

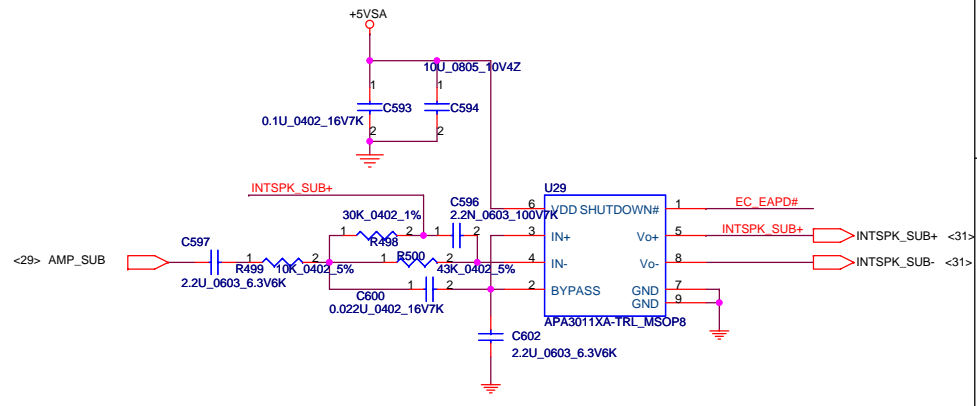
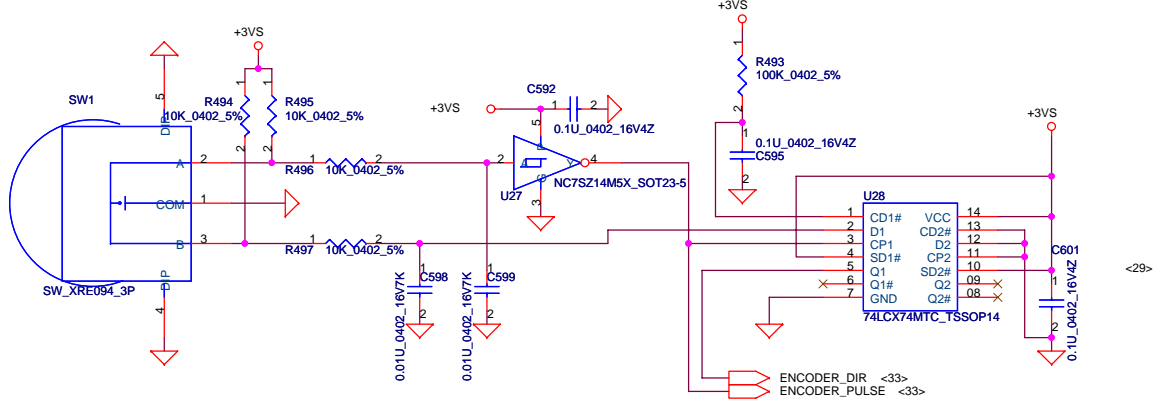


Pin2 /SD should be tied to 5V always and mute pin controlled by EC_EAPD



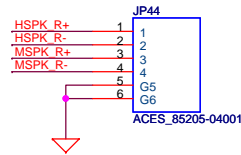
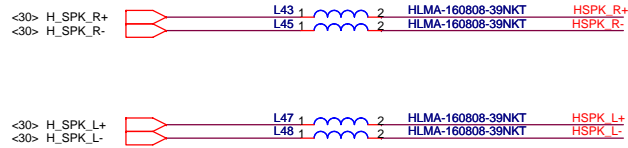
Volume Control

APA3011 Subwoofer Amplifier

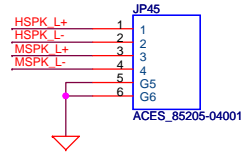
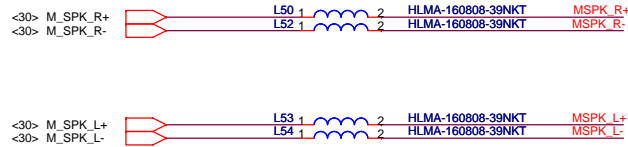


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Size	Document Number	Rev		
Custom	LA-3441P	0.1		
Date:	Friday, September 22, 2006	Sheet	30	of 48

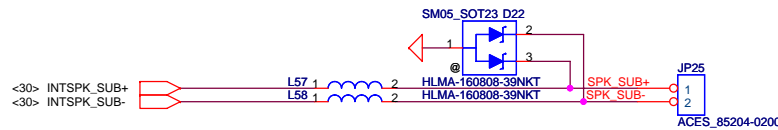
Tweeter Conn.



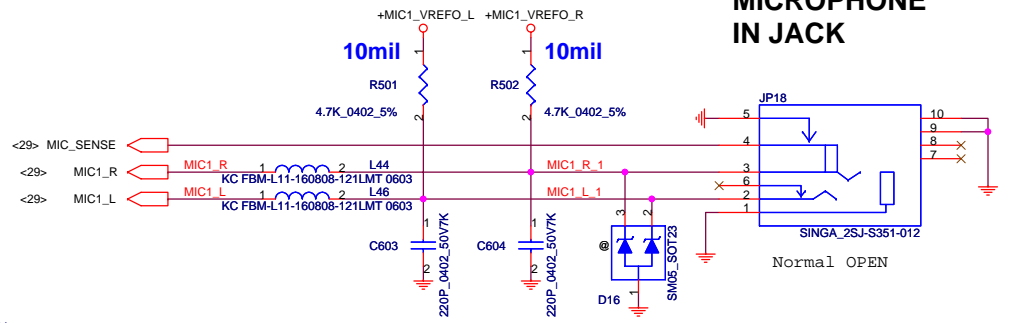
Medium SPK Conn.



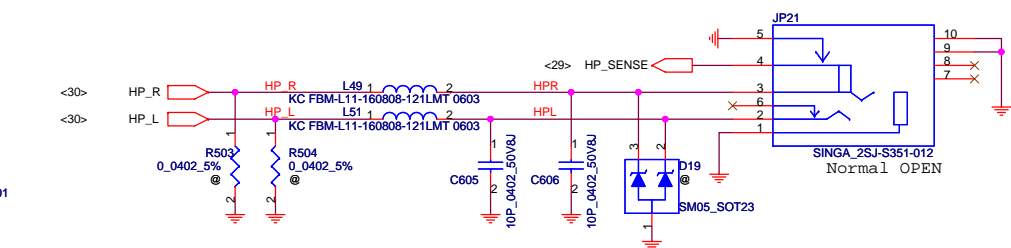
Sub-woofer Conn.



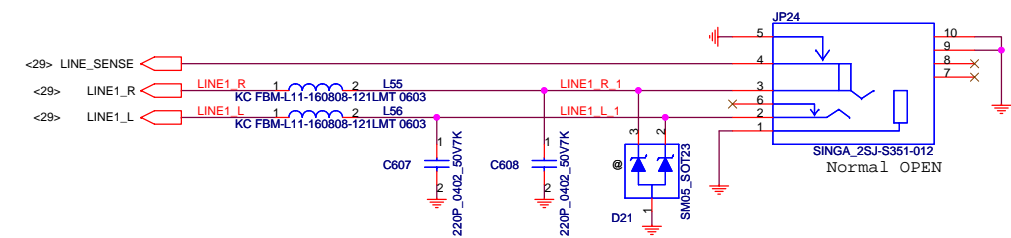
MICROPHONE IN JACK



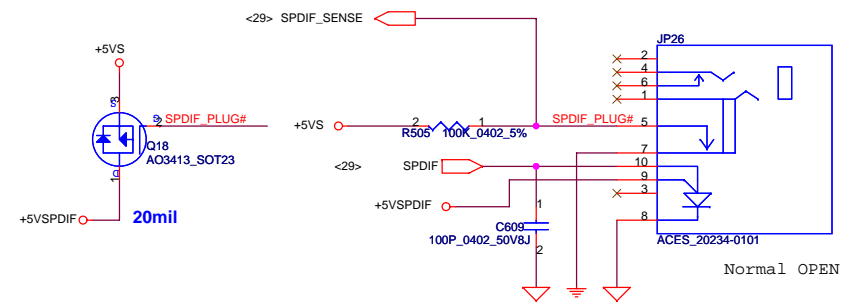
HEADPHONE OUT JACK



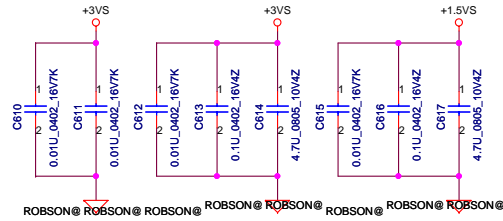
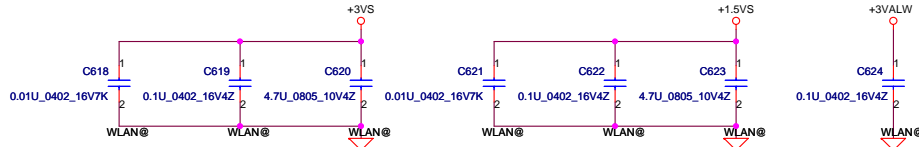
LINE IN JACK



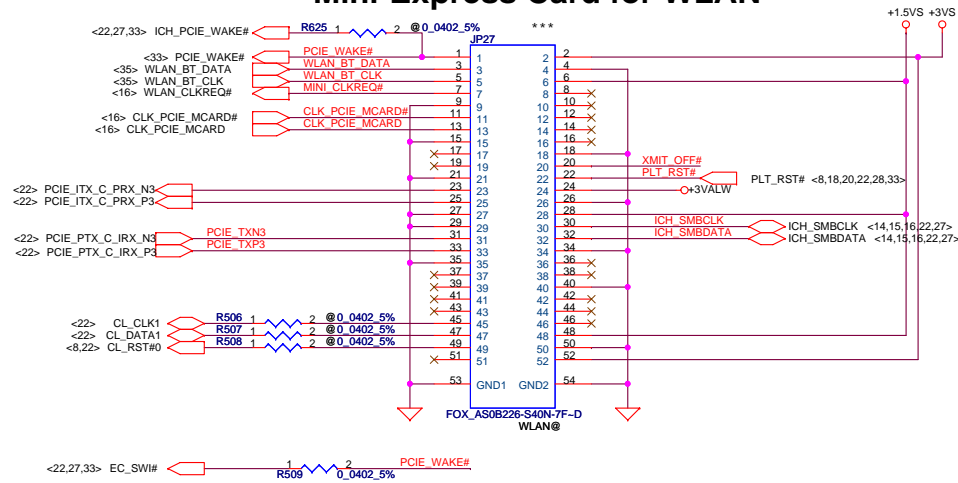
S/PDIF OUT JACK



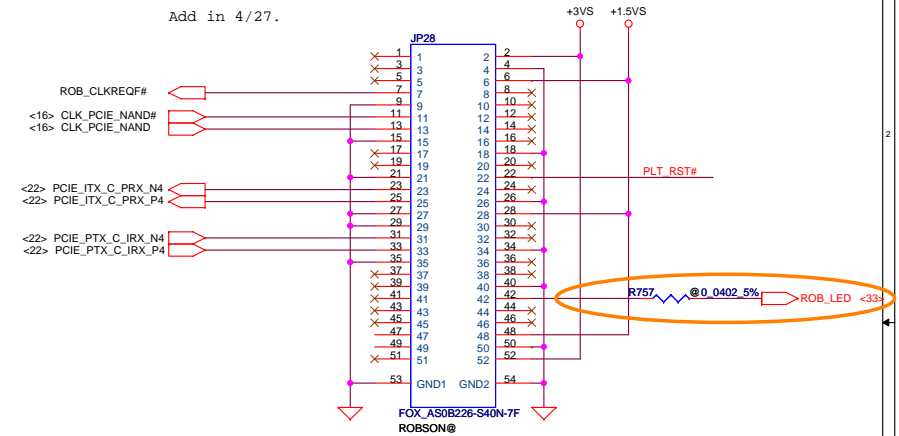
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/06/30	Deciphered Date	2007/06/30	Title <Title> Audio Jack/MIC/SPDIF
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Date:	Friday, September 22, 2006	Sheet	31 of 48	



Mini-Express Card for WLAN



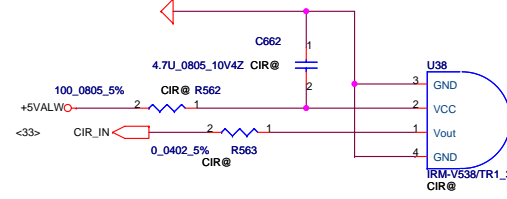
NAND mini Card(Robson support)



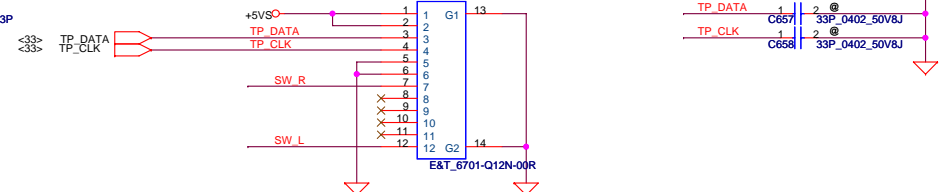
TP Button



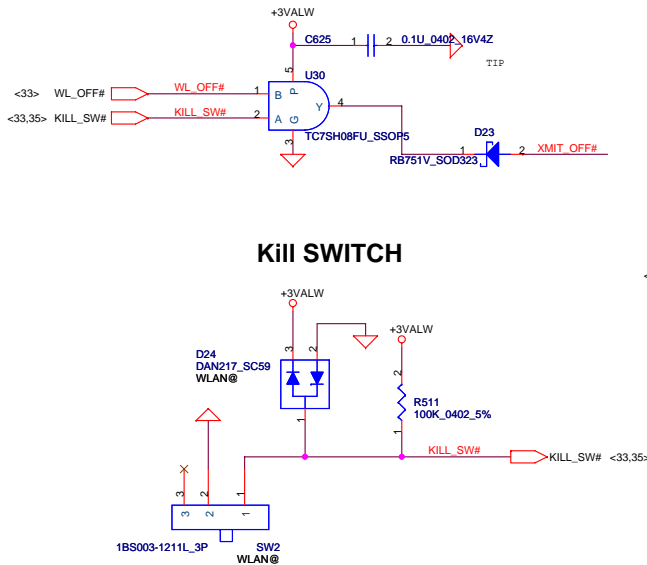
CIR



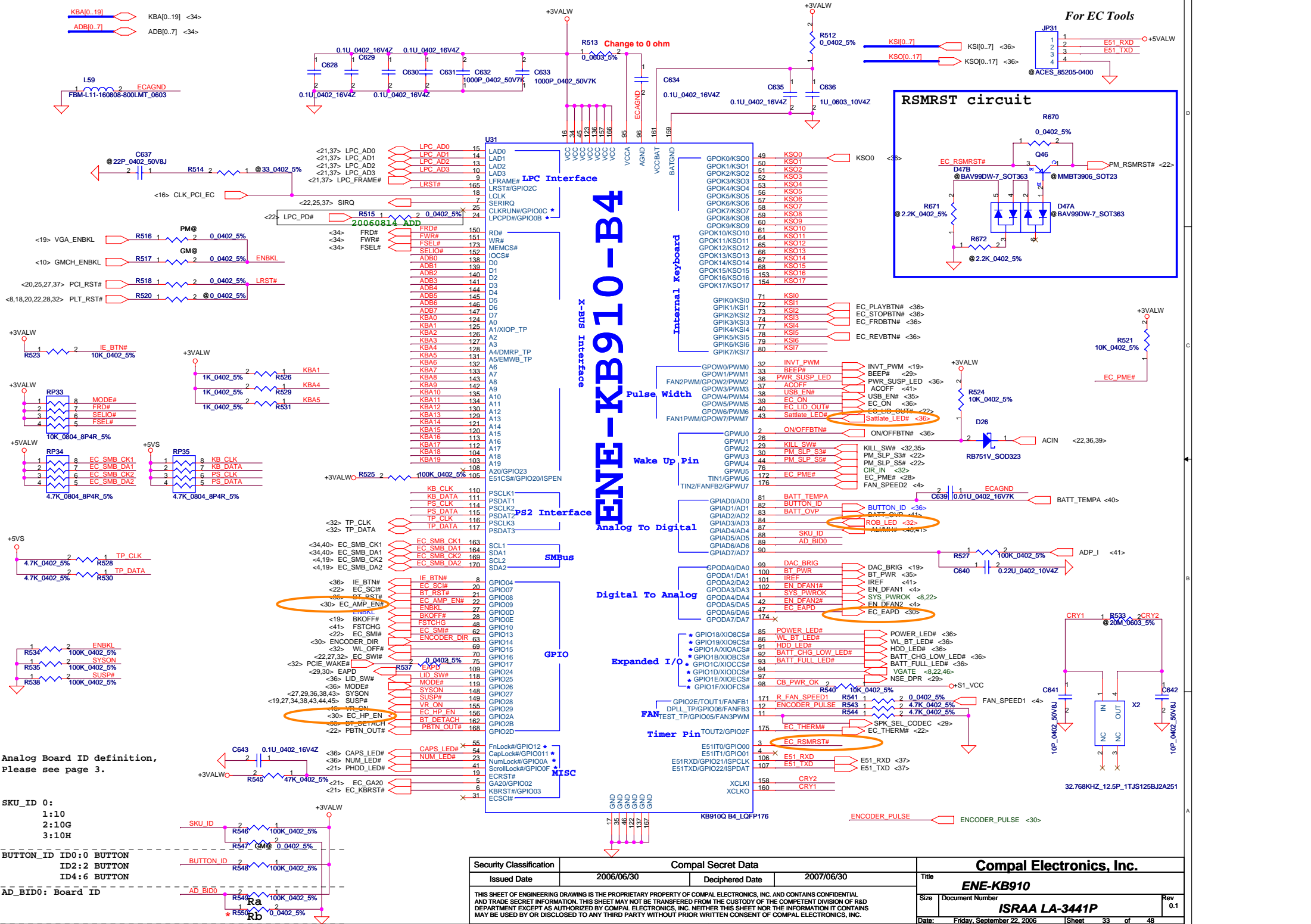
TP CONN.

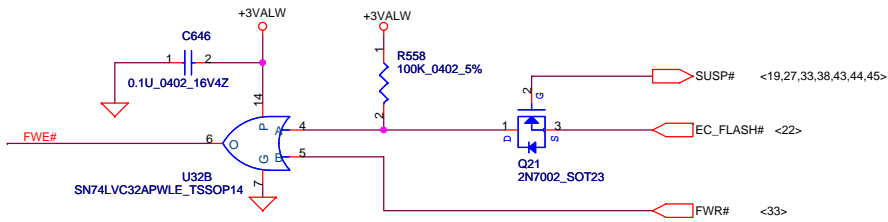
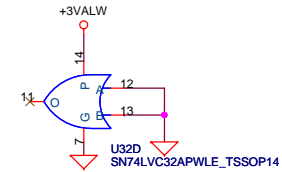
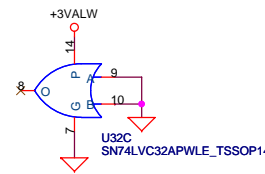
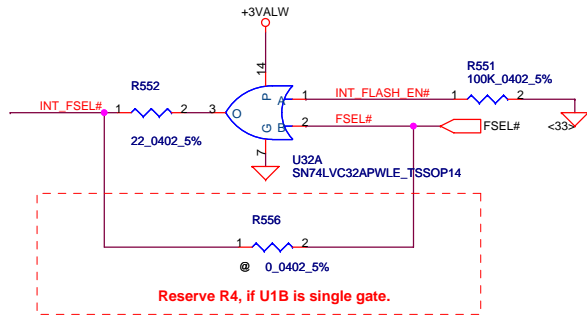


Kill SWITCH

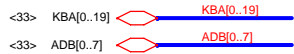


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Issued Date	2006/06/30	Deciphered Date	2007/06/30	Mini-Card/CIR/TP Conn	
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				ISRAA LA-344IP	Rev 0.1
Date:				Friday, September 22, 2006	Sheet 32 of 48

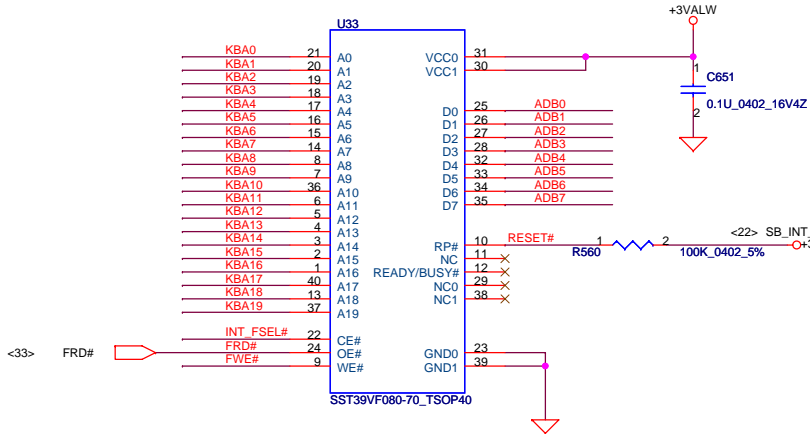




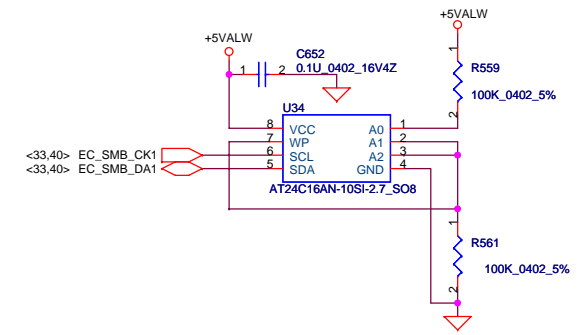
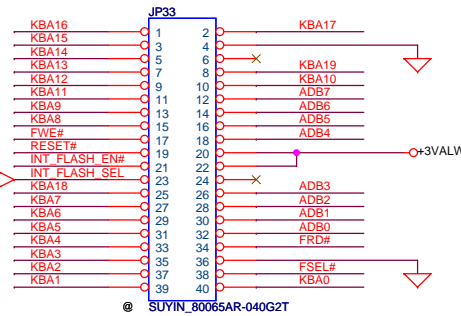
Module ID
 Indication for polarity of reset
 Reset input High Active --> Low ,
 Reset input Low Active --> Open



1MB Flash ROM

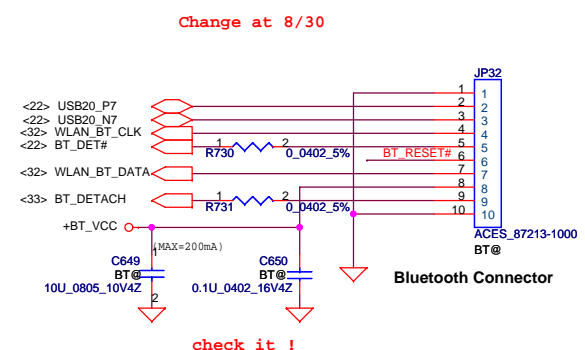
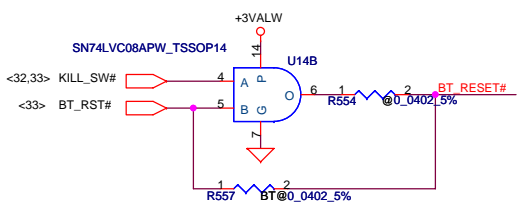
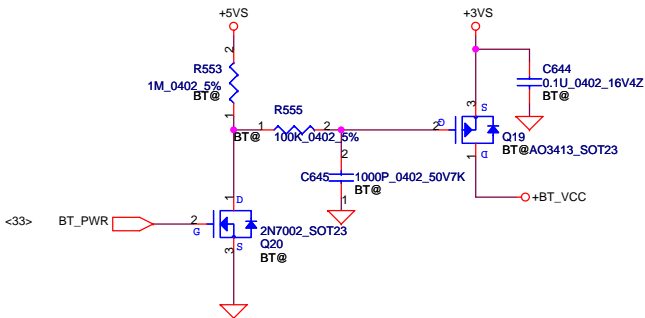


1MB ROM Socket



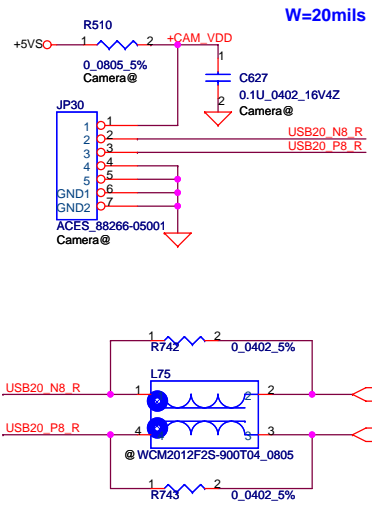
Security Classification	Compal Secret Data		Title	
Issued Date	2006/06/30	Deciphered Date	2007/06/30	BIOS I/F
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				Document Number
				ISRAA LA-3441P
				Rev
				0.1
Date:		Friday, September 22, 2006		Sheet
		34		of
		48		

BlueTooth Interface

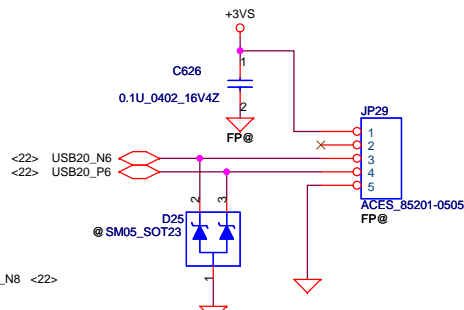


Change at 8/30

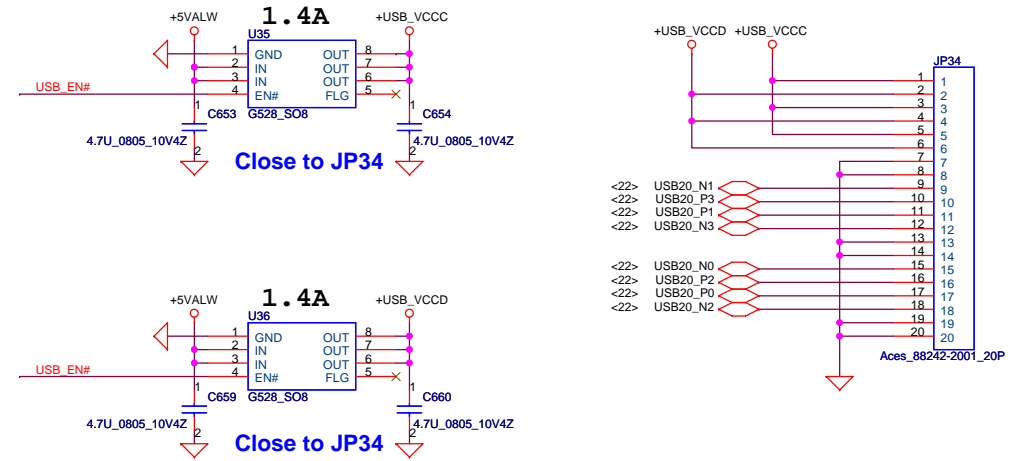
Int. Camera Conn



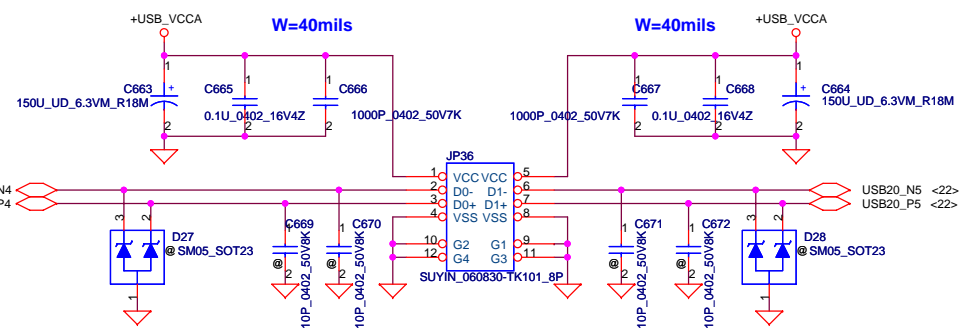
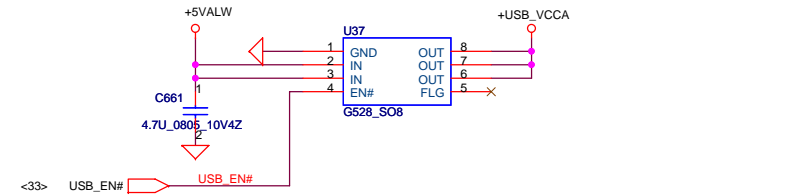
Finger printer Conn



USB Board Right side 2x2 Port

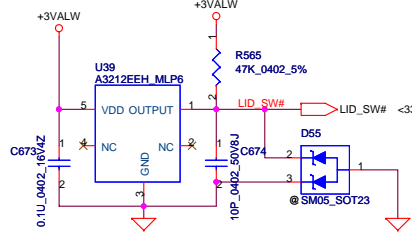


USB Conn Left side 1x2 Port

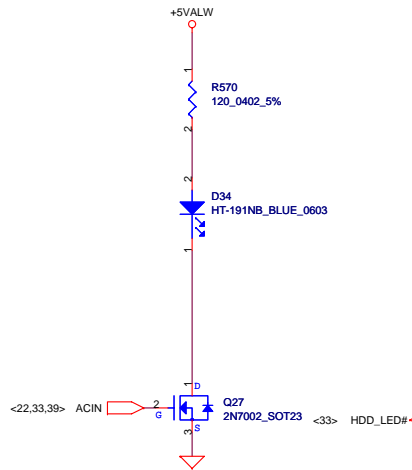


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Size	Document Number	ISRAA LA-3441P		Rev	0.1
Date:	Friday, September 22, 2006	Sheet	35	of	48

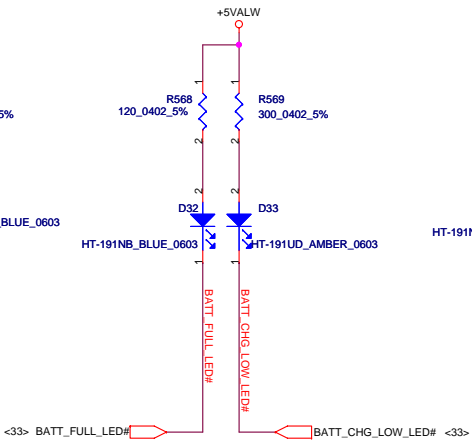
Lid SW



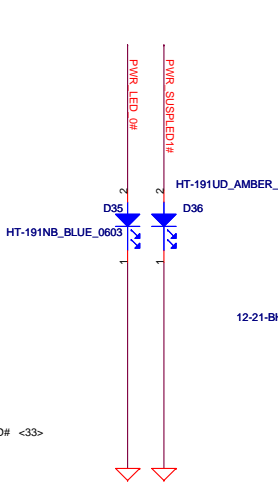
HDD LED



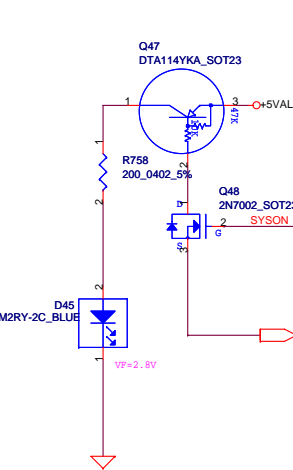
BATT CHARGE/FULL LED



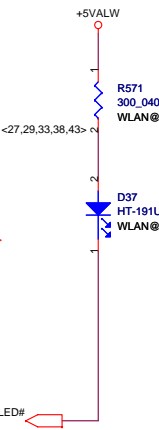
POWER/SUSPEND LED



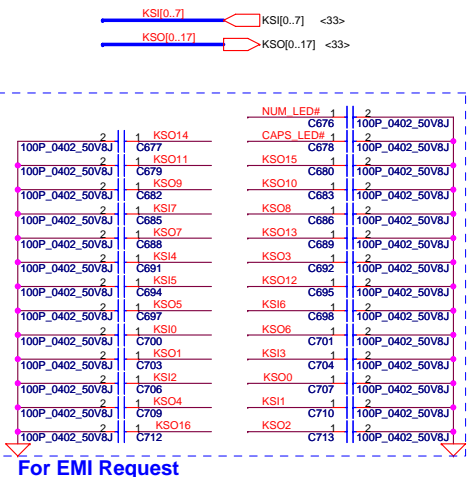
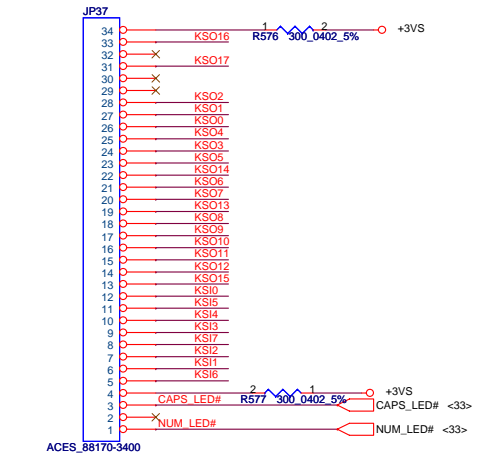
Satellite logo LED



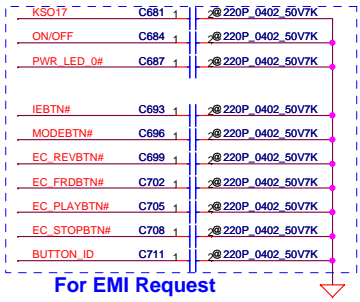
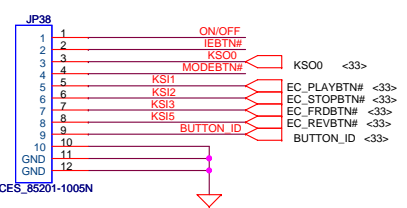
WL&BT LED



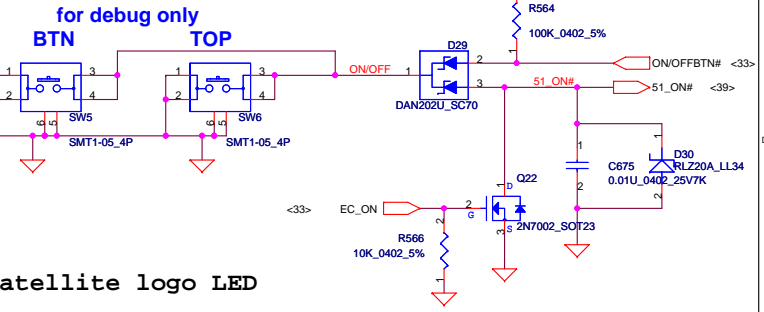
KEYBOARD CONN.



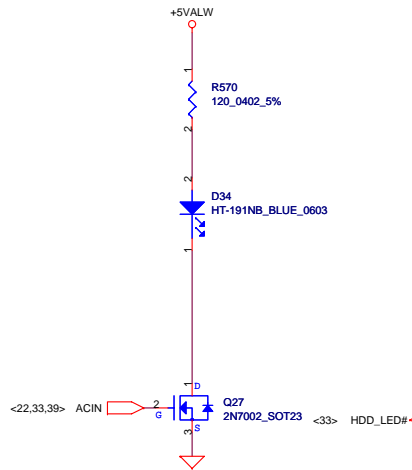
SW/LED Connector



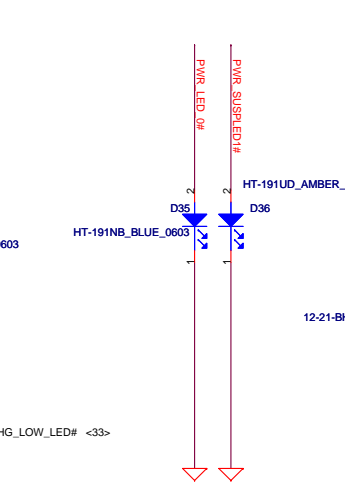
ON/OFF BUTTON



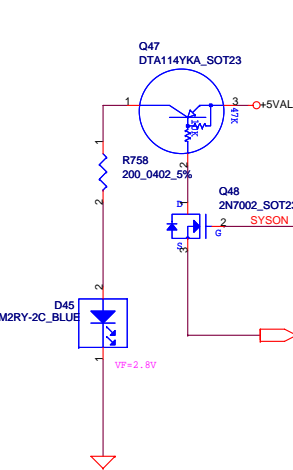
AC IN LED



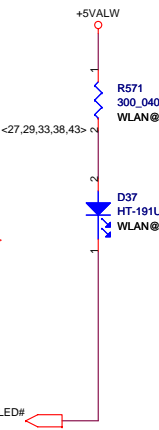
POWER/SUSPEND LED



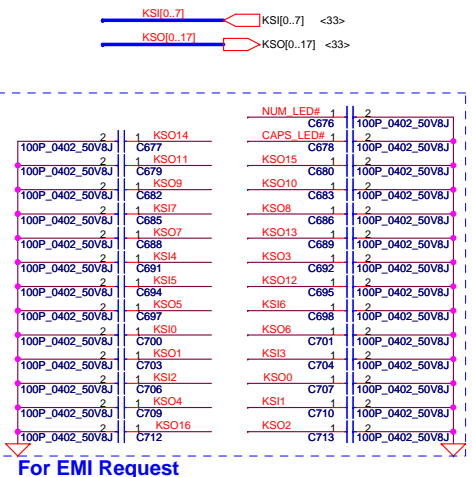
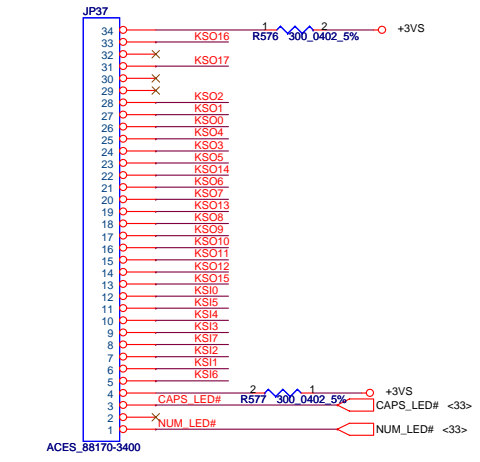
Satellite logo LED



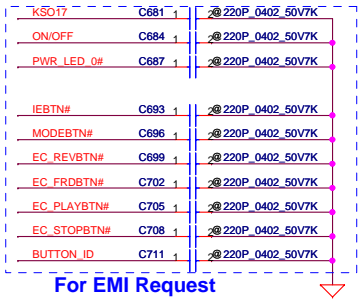
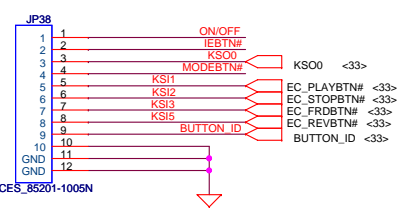
WL&BT LED



KEYBOARD CONN.



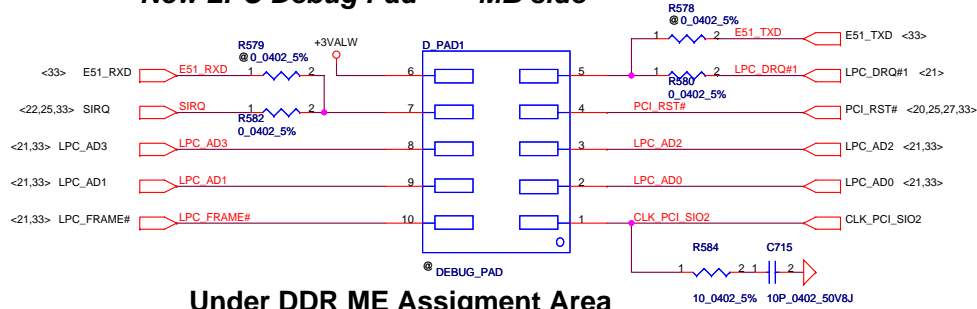
SW/LED Connector



20070718 change new KB define

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				ISRAA LA-3441P	
Date: Friday, September 22, 2006				Rev 0.1	
				Sheet 36 of 48	

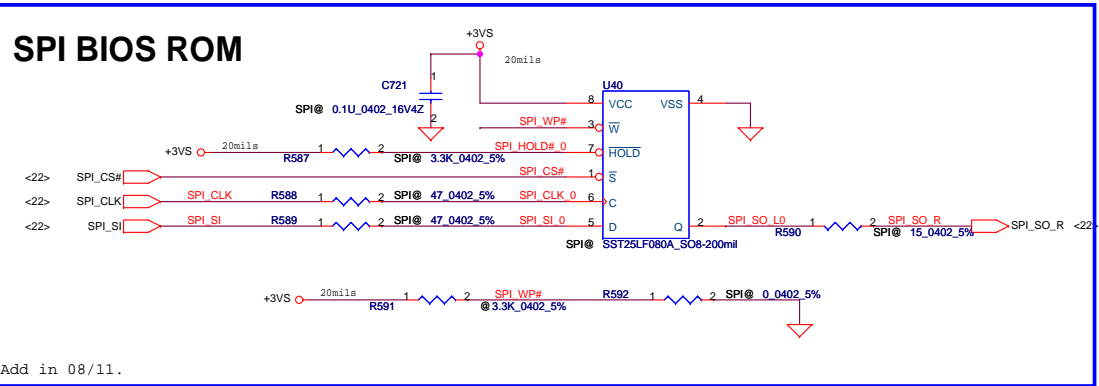
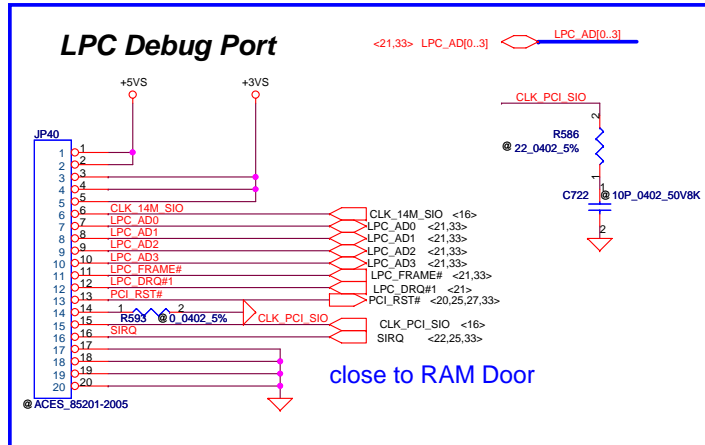
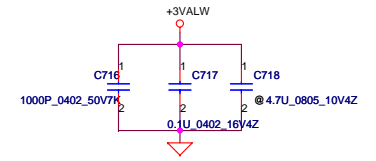
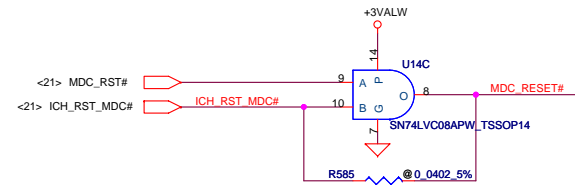
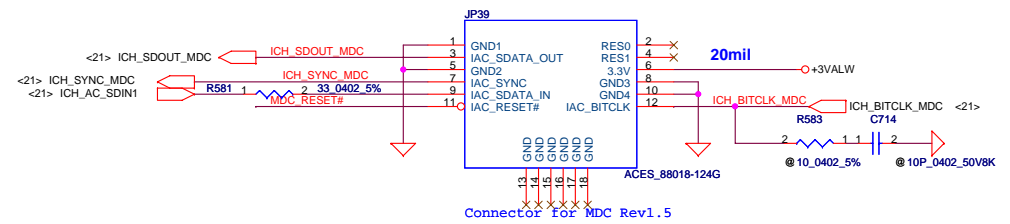
New LPC Debug Pad ---- MB side



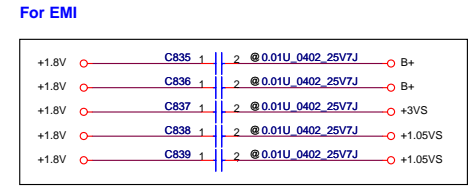
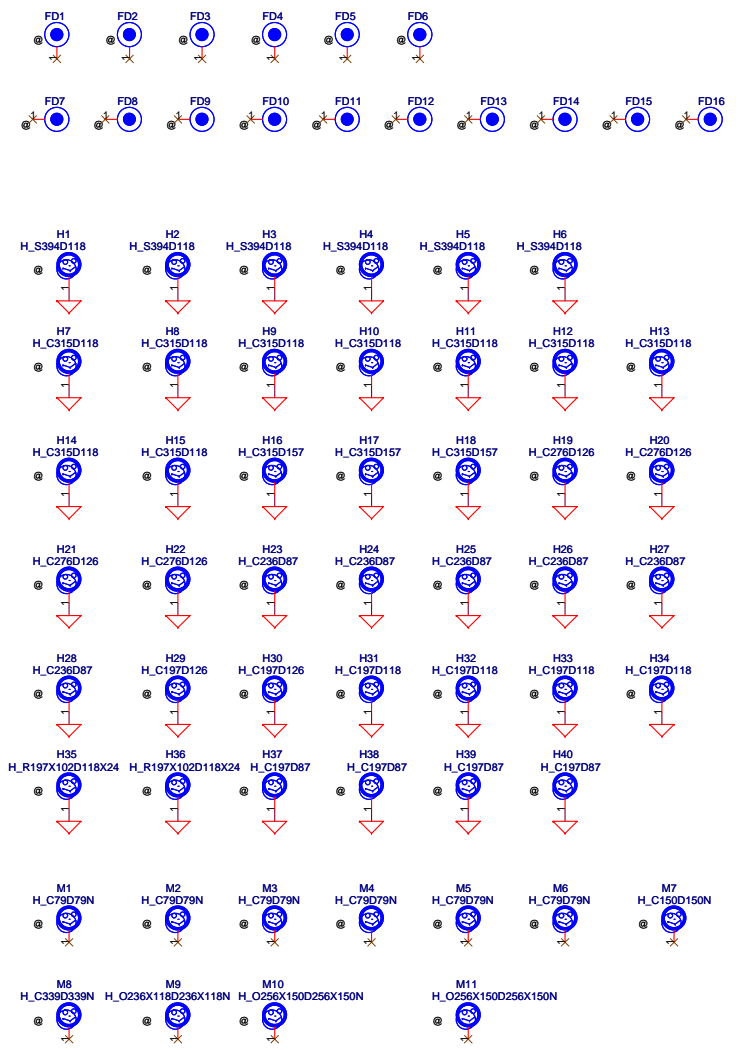
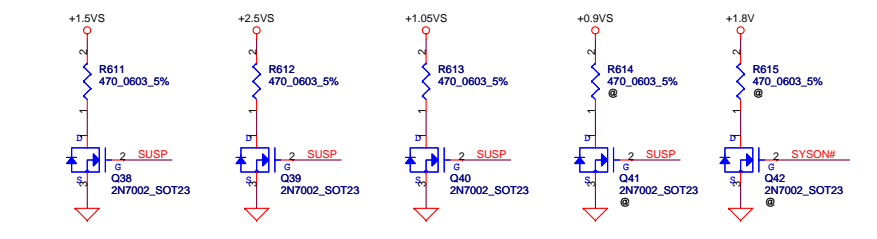
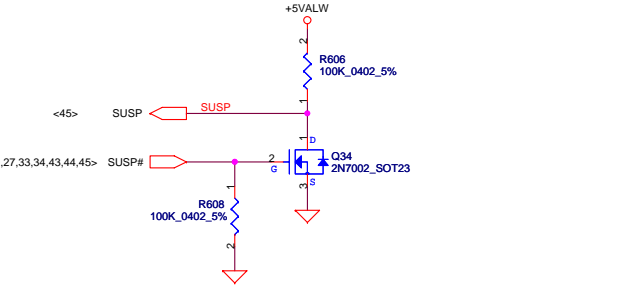
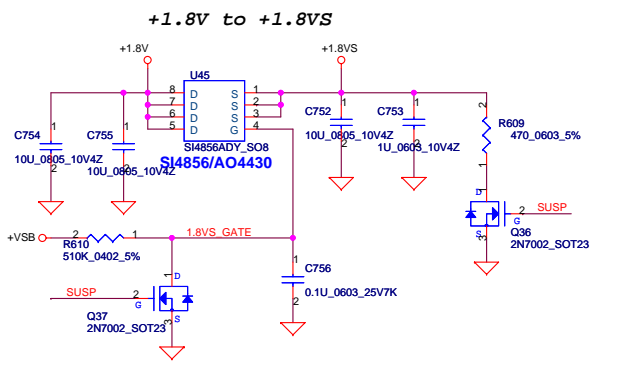
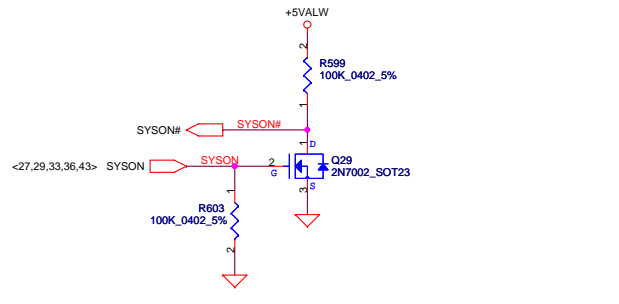
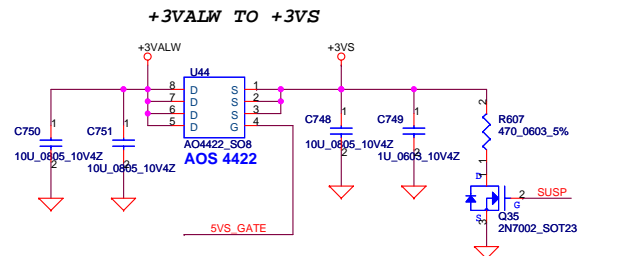
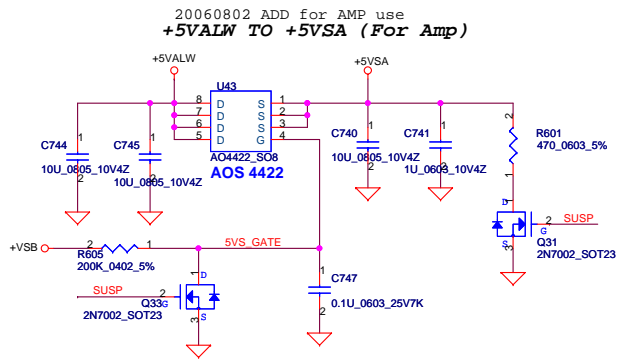
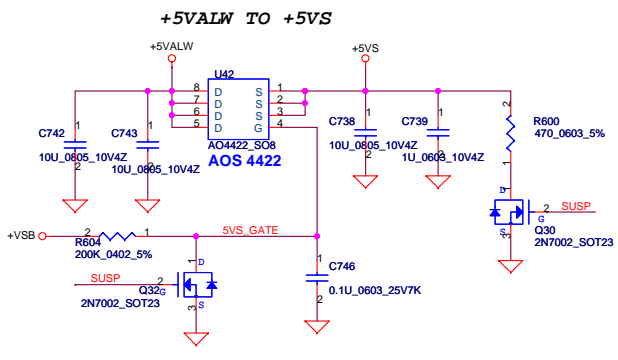
Under DDR ME Assignment Area

Keep Resistor near Debug Pad and in the same side
Reverse side DIMM ---- Pin 1 keep away DIMM

MDC Conn.

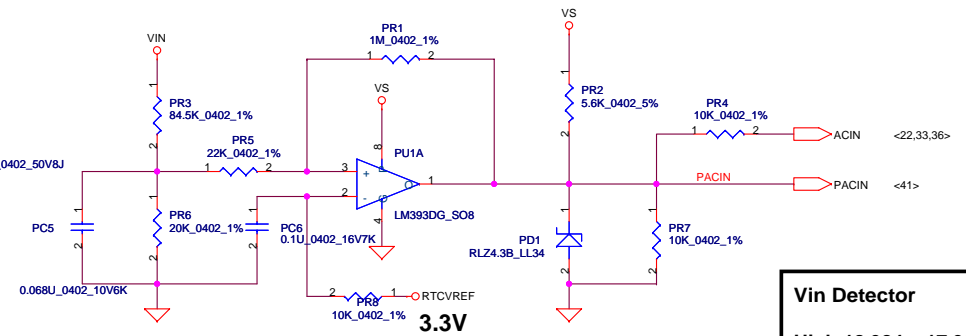
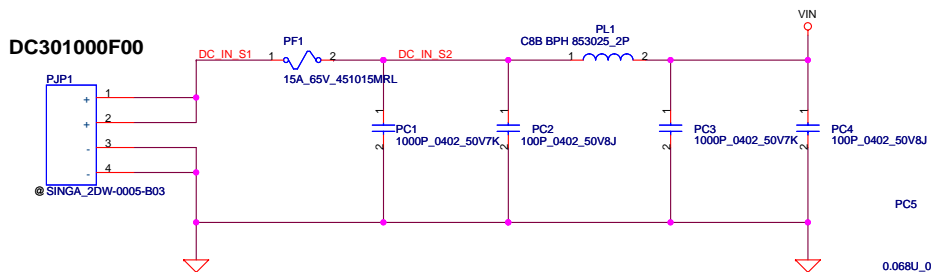


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				ISRAAA LA-3441P
				Rev
				0.1
				Date:
				Friday, September 22, 2006
				Sheet
				37
				of
				48

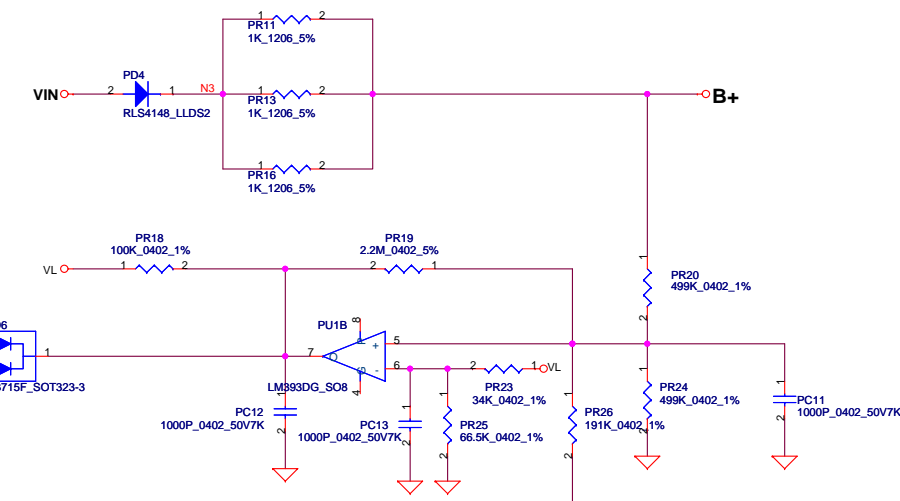
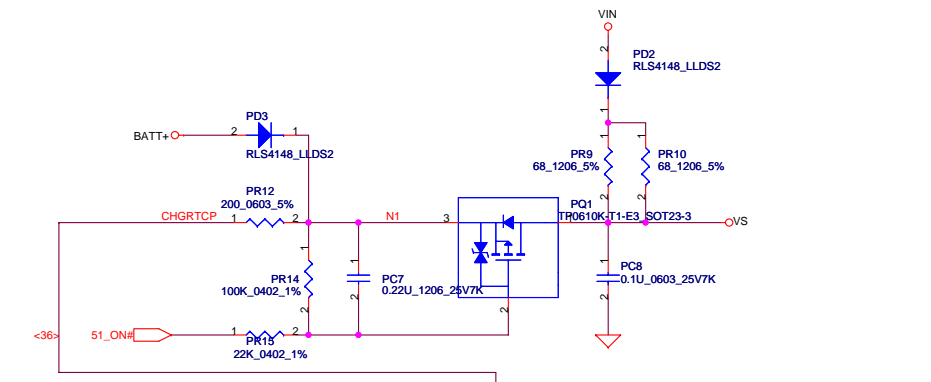


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				Date:	Friday, September 22, 2006
				Sheet	38 of 48

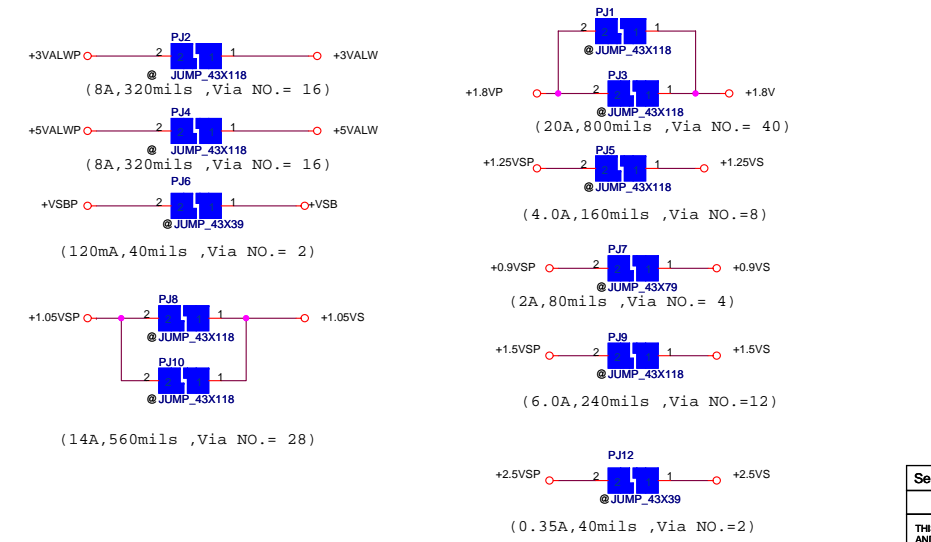
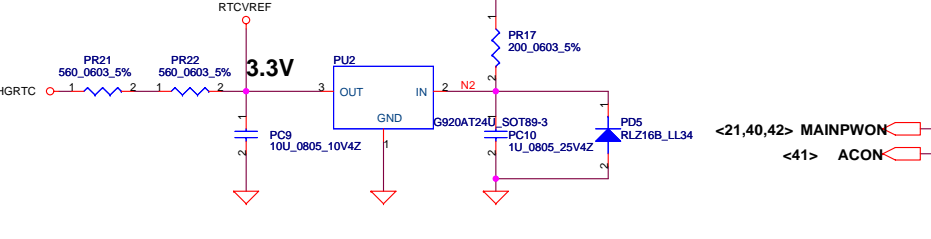
DC301000F00



Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976

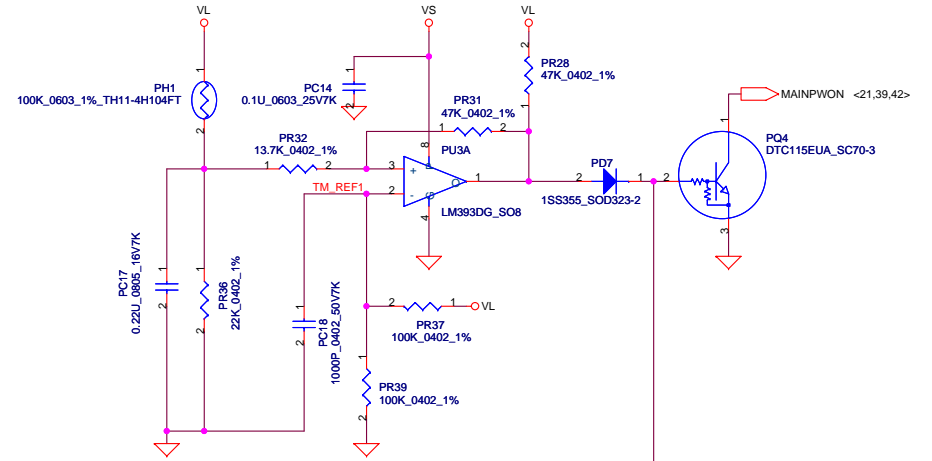


Precharge detector
 15.97V/14.84V FOR
 ADAPTOR

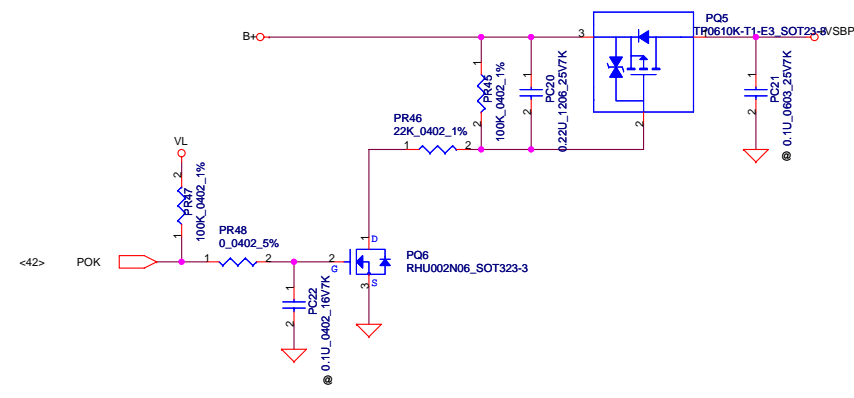
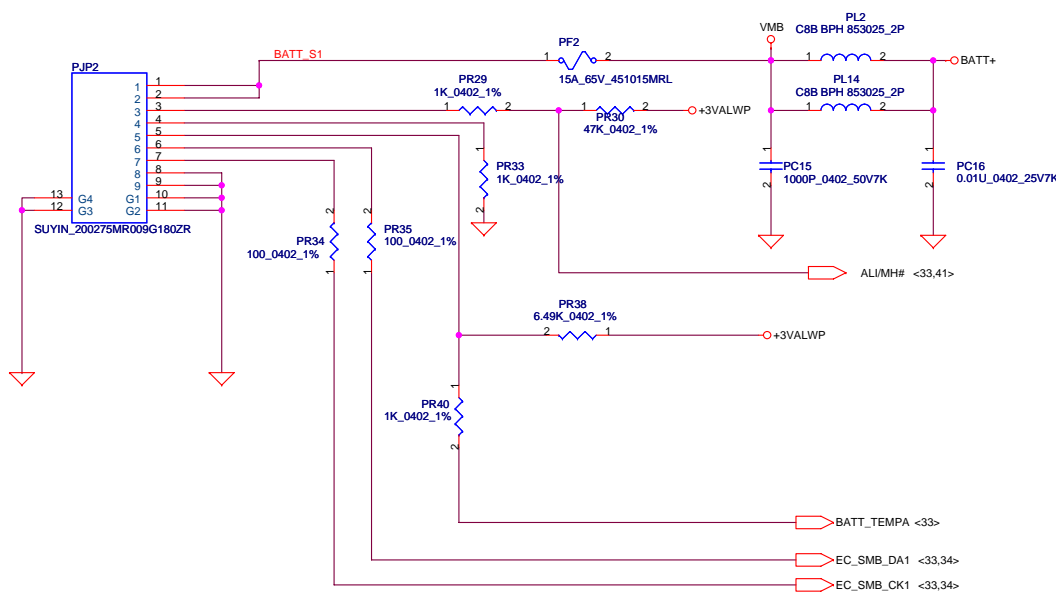
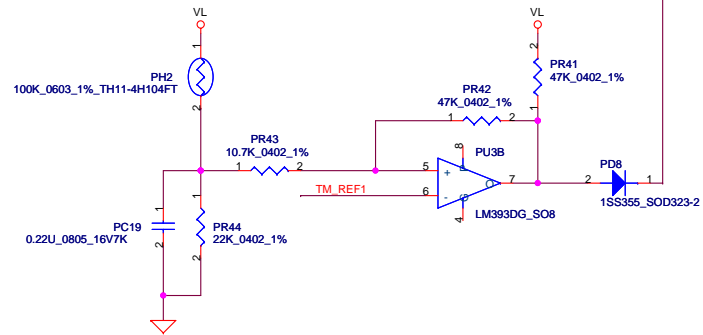


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Size	Document Number				Rev
					0.1
Date:	Friday, September 22, 2006	Sheet	39	of	48

PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C

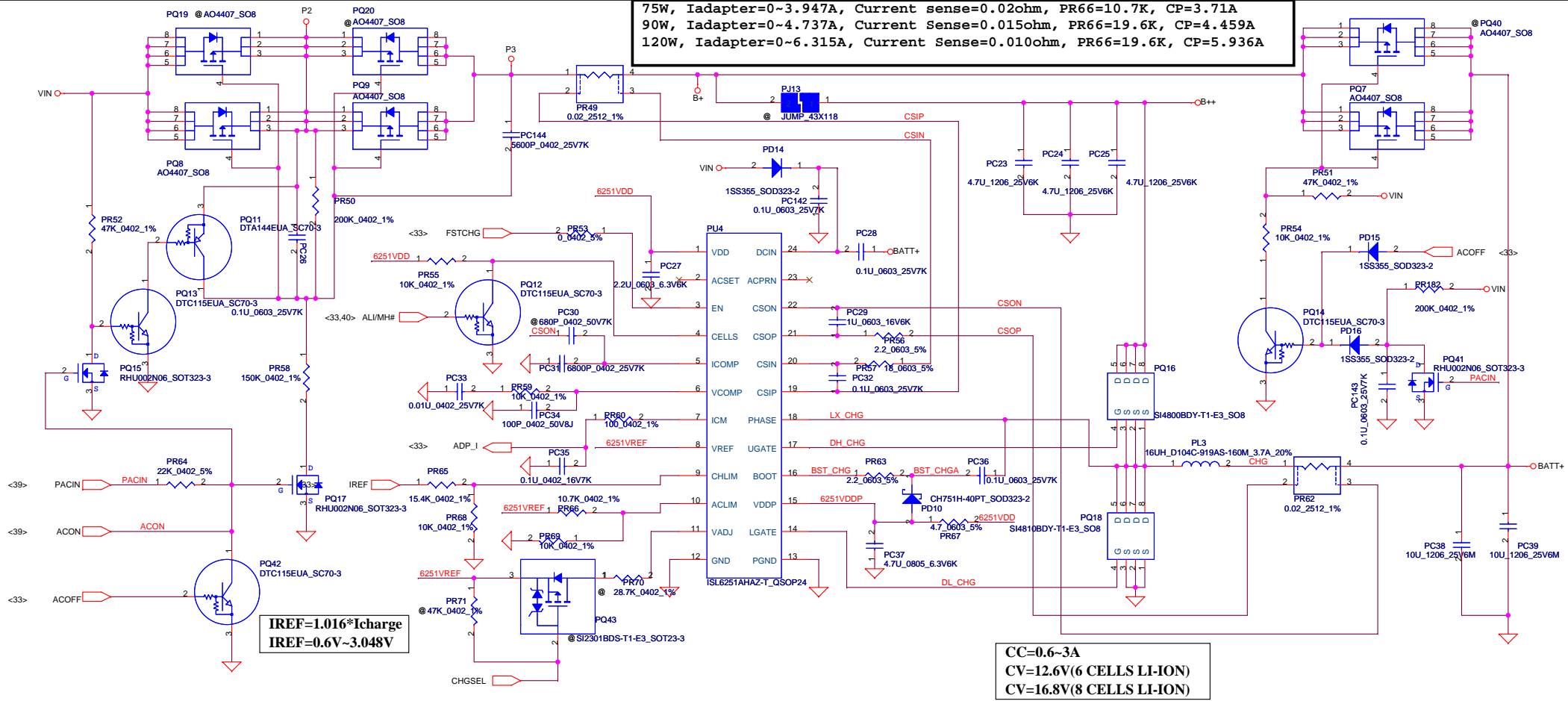


PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 45 degree C



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Size	Document Number			Rev	
Date:	Friday, September 22, 2006	Sheet	40	of	48

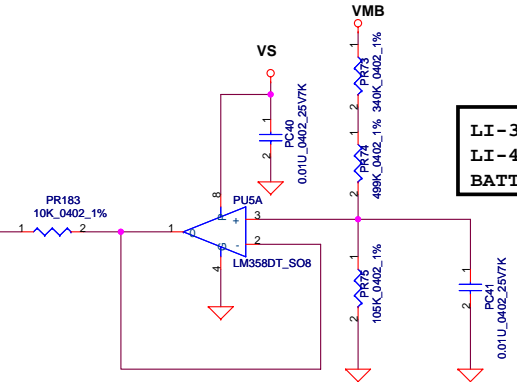
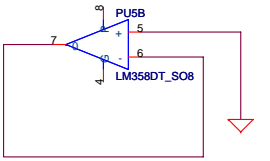
75W, Iadapter=0~3.947A, Current sense=0.02ohm, PR66=10.7K, CP=3.71A
 90W, Iadapter=0~4.737A, Current Sense=0.015ohm, PR66=19.6K, CP=4.459A
 120W, Iadapter=0~6.315A, Current Sense=0.010ohm, PR66=19.6K, CP=5.936A



$I_{REF} = 1.016 * I_{charge}$
 $I_{REF} = 0.6V \sim 3.048V$

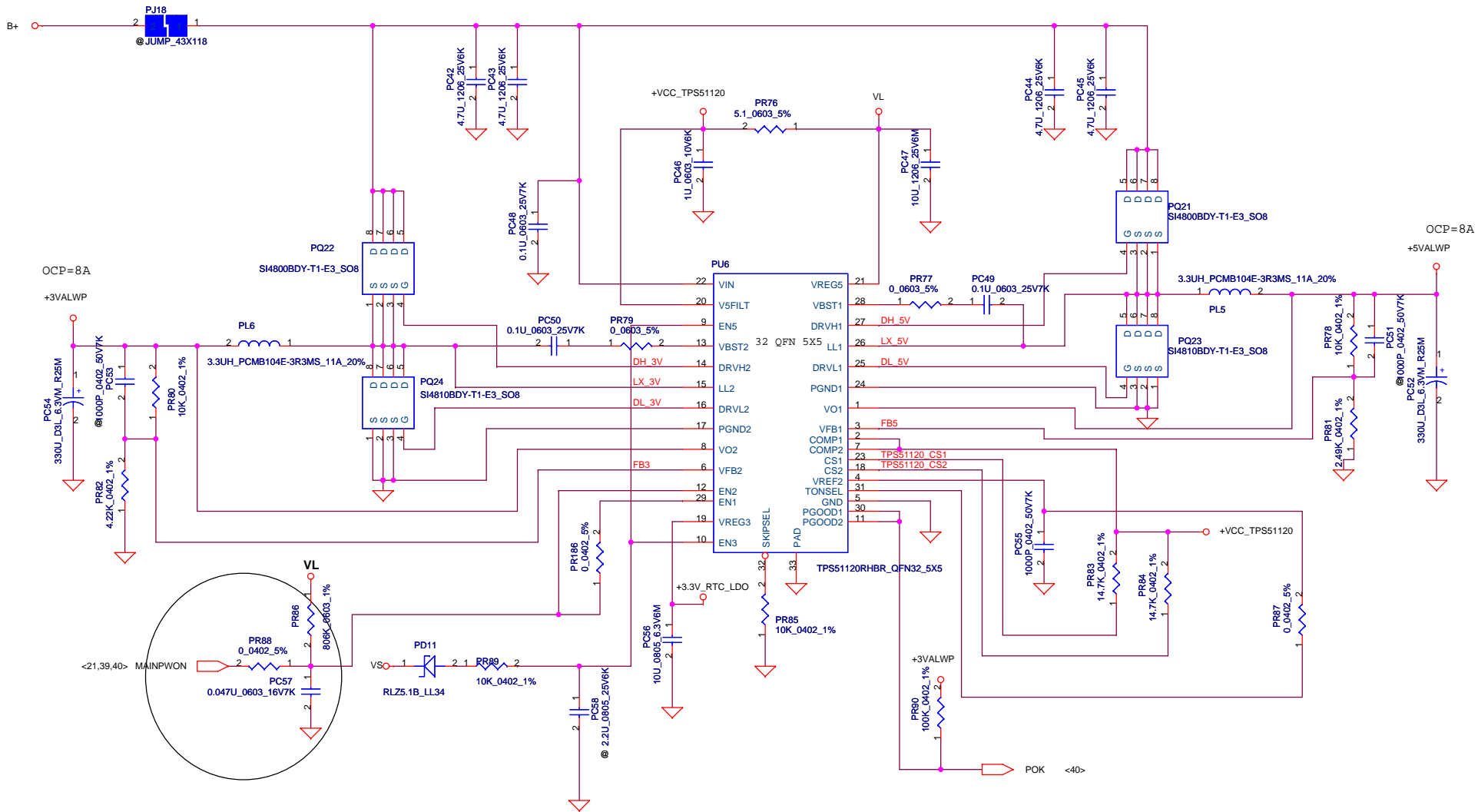
$CC = 0.6 \sim 3A$
 $CV = 12.6V (6 \text{ CELLS LI-ION})$
 $CV = 16.8V (8 \text{ CELLS LI-ION})$

BATT Type	ALI/MH#	CELLS	Charge Current	IREF
4S2P	0V	HIGH	3A	3.048V
3S2P	2.5V	LOW	3A	3.048V
4S1P	0V	HIGH	1.5A	1.524V
Trickle Charge = 600mA				0.61V



LI-3S : 13.5V --- BATT-OVP=1.5V
 LI-4S : 18V --- BATT-OVP=2V
 BATT-OVP = 0.111 * BATT+

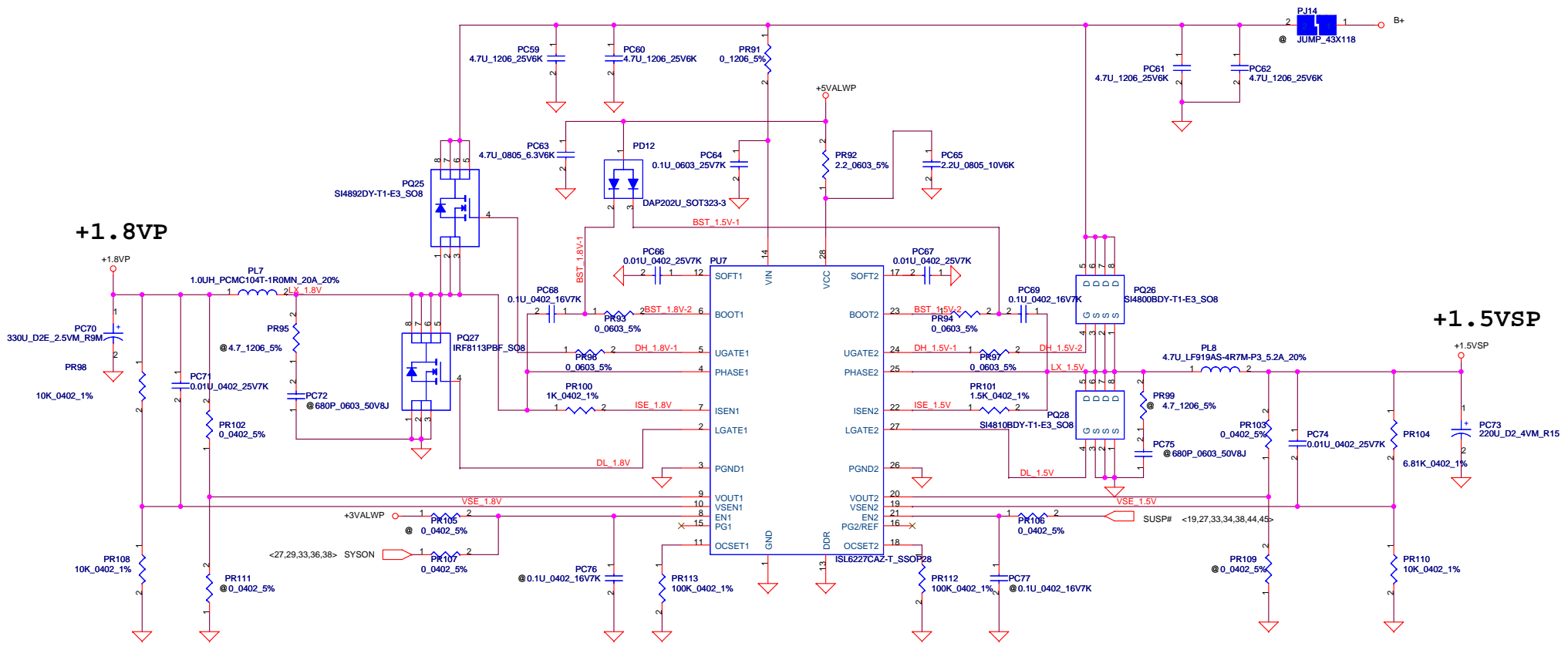
BATT Type	Charging Voltage (0x15)	ALI/MH#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V



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Date:	Friday, September 22, 2006	Sheet	42	of	48

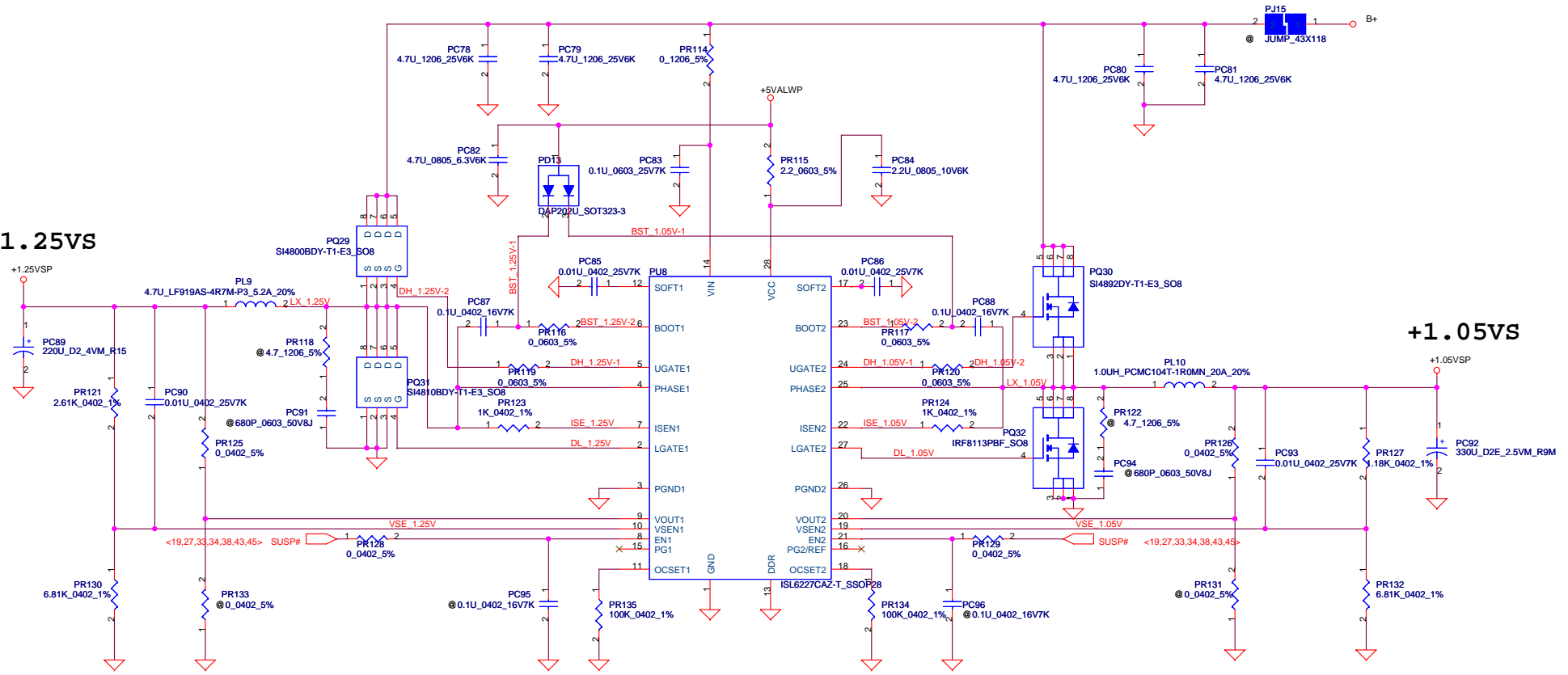
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 Rev: 0.1
 Date: Friday, September 22, 2006
 Sheet: 42 of 48



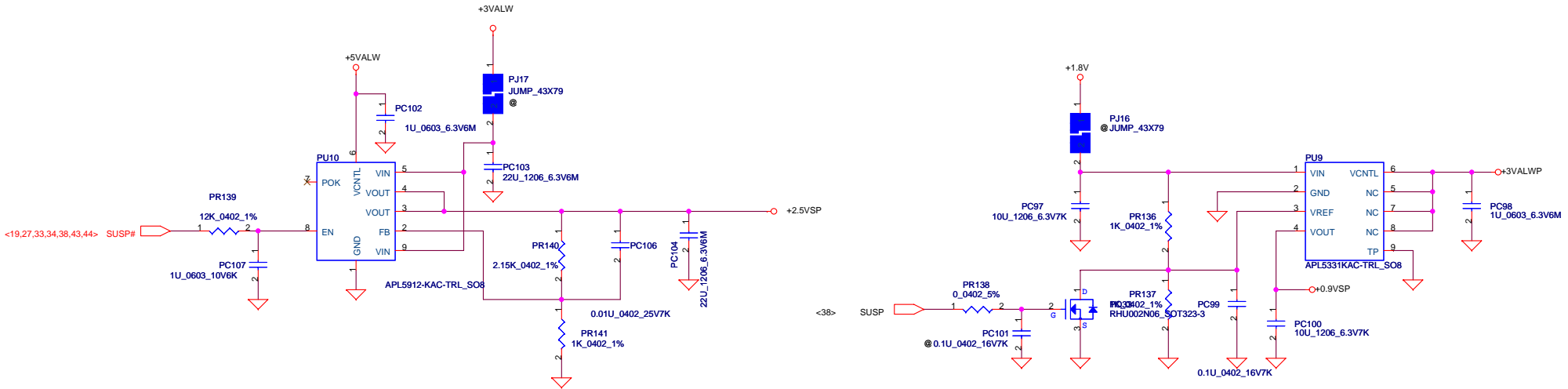
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				Date:	Friday, September 22, 2006	Sheet 43 of 48

+1.25VS

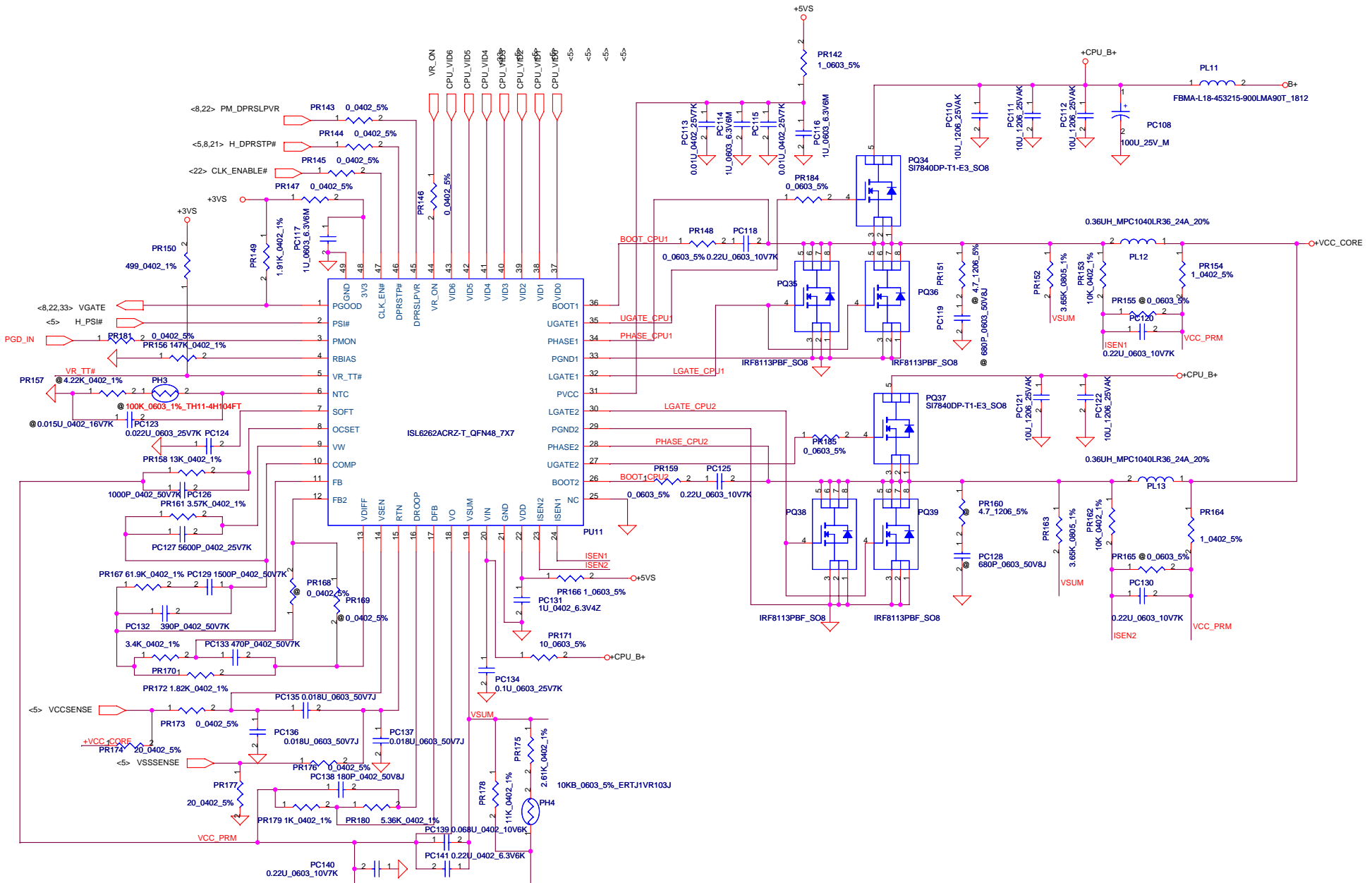


+1.05VS

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Size	Document Number			Rev
				0.1
Date:	Friday, September 22, 2006	Sheet	44	of 48



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				Date:	Friday, September 22, 2006
				Sheet	45 of 48
				Rev	0.1



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Compal Electronics, Inc. +CPU_CORE		
Size	Document Number	Rev
Custom	Cleveland	0.1
Date:	Friday, September 22, 2006	Sheet 46 of 48

HW4 Product Improvement Record (P.I.R.)

Phase: A to B

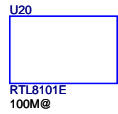
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Writer: Timo Teng

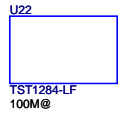
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				Date: Thursday, September 21, 2006	Sheet 47 of 48

LAN



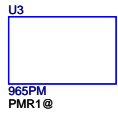
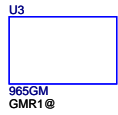
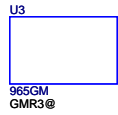
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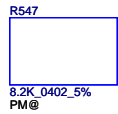
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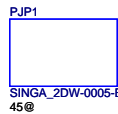
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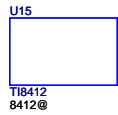
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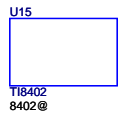
DC-JACK



8412



8402



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				Size	Document Number
Date:	Thursday, September 21, 2006	Sheet	48	of	48